NATIONAL TECHNICAL UNIVERSITY OF ATHENS

SCHOOL OF ELECTRICAL AND COMPUTER ENGINEERING

ELECTRIC POWER DIVISION



Solid-State Circuit Breaker for Alternating Current Applications

DIPLOMA THESIS

by

STEFANOS CHRONOPOULOS

Supervisor: Antonios Antonopoulos
Associate Professor N.T.U.A.

Athens, October 2026

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Περίληψη

Η παρούσα διπλωματική εργασία μελετά τους διακόπτες στερεάς κατάστασης (SSCB) σε συστήματα εναλλασσόμενου ρεύματος. Η αυξανόμενη παρουσία ηλεκτρονικών ισχύος, η ηλεκτροκίνηση και η διείσδυση κατανεμημένης παραγωγής δημιουργούν ανάγκες ταχύτερης και ελεγχόμενης προστασίας. Η χρήση ημιαγωγών επιτρέπει γρήγορη διακοπή, αλλά εισάγει απαιτήσεις ως προς τις απώλειες αγωγής, τον περιορισμό της υπέρτασης και τη διαχείριση της ενέργειας.

Αρχικά αναλύονται τα σφάλματα σε δίκτυα εναλλασσόμενου ρεύματος και συγκρίνονται οι ηλεκτρομηχανικές, υβριδικές και αμιγώς ηλεκτρονικές τεχνολογίες διακοπής. Εξετάζονται οι ημιαγωγοί πυριτίου και ευρέος ενεργειακού διακένου, οι αμφίδρομες τοπολογίες και τα κυκλώματα οδήγησης, ανίχνευσης σφαλμάτων και προστασίας.

Σε μονοφασικά και τριφασικά μοντέλα Simulink μελετώνται η αποκοπή σφαλμάτων, ο ενεργός περιορισμός ρεύματος και η ενέργεια που απορροφούν τα βαρίστορ οξειδίου μετάλλου (MOV). Τα αποτελέσματα δείχνουν ταχεία διακοπή πριν από τον φυσικό μηδενισμό του ρεύματος και σημαντική αύξηση της σωρευτικής ενέργειας των MOV κατά τις επαναλαμβανόμενες μεταγωγές. Μια ελεγχόμενη διαδρομή ελεύθερης εκφόρτισης εξετάζεται σε προσομοίωση, ώστε να μεταφέρει ενέργεια σε αντίσταση και να μειώνει την καταπόνησή τους. Στο τριφασικό σύστημα εξετάζονται επίσης η κοινή αποκοπή, η διαφορετική καταπόνηση ανά φάση και η προστασία τοπικής σύγχρονης παραγωγής.

Η μελέτη συμπληρώνεται με πειράματα σε εμπορικές πλακέτες της onsemi, με εξωτερικό έλεγχο μέσω μικροελεγκτή. Εξετάζονται η αυτόματη αποκοπή υπερέντασης, η παράλληλη λειτουργία, η καθυστέρηση της ψηφιακής αλυσίδας και η σύγκριση με ηλεκτρομηχανικό επαφέα. Επιβεβαιώνεται η γρήγορη αποκοπή ανεξάρτητα από τον φυσικό μηδενισμό. Στην παράλληλη λειτουργία, ο καλός διαμοιρασμός κατά την αγωγή συνοδεύεται από άνισα εξωτερικά ρεύματα κατά τη σβέση, χωρίς να απομονώνεται η κυρίαρχη αιτία. Η διαχείριση ενέργειας και ο συντονισμός της μεταβατικής απόκρισης αναδεικνύονται ως βασικά κριτήρια σχεδιασμού. Ως συνέχεια προτείνονται η πειραματική δοκιμή της διαδρομής εκφόρτισης και η διερεύνηση της παράλληλης σβέσης.

Λέξεις κλειδιά: *Διακόπτης στερεάς κατάστασης, προστασία εναλλασσόμενου ρεύματος, SiC, αποκοπή σφάλματος, περιορισμός ρεύματος, ενέργεια MOV, παράλληλη λειτουργία.*

Abstract

This thesis investigates Solid-State Circuit Breakers (SSCBs) for alternating current (AC) power systems. The increasing use of power electronics, electrification and distributed renewable generation creates a need for fast, controllable fault protection. SSCBs address this need through semiconductor switching, while introducing challenges related to conduction losses, voltage clamping and energy management.

The work reviews AC fault behavior and compares electromechanical, hybrid and solid-state interruption technologies. Silicon and wide-bandgap power devices are assessed in terms of their static and dynamic characteristics, voltage and current ratings, and suitability for SSCB applications. The analysis also examines bidirectional AC topologies, gate driving, fault detection and auxiliary protection circuits.

Single-phase and three-phase Simulink models are used to study fault interruption, current limiting and the energy absorbed by metal-oxide varistors (MOVs). The results demonstrate fast interruption before the natural current zero and show that repeated switching during current limiting can substantially increase cumulative MOV energy. A controlled freewheeling path is investigated in simulation to divert energy to a resistive branch and reduce MOV stress. The three-phase analysis also considers common tripping, unequal loading of the phase clamping elements and protection of local synchronous generation.

Laboratory experiments on commercial onsemi SSCB evaluation boards complement the simulations. The tests include manual and processor-based control, automatic overcurrent interruption, parallel operation, response-time measurement and comparison with an electromechanical contactor. An external controller acquires board measurements through SPI and implements the protection logic. The experiments confirm rapid interruption independently of the natural current zero and quantify the latency of the digital control chain. Parallel operation gives close steady-state current sharing but unequal external branch currents during turn-off despite a common command; the dominant cause is not isolated. Overall, the work identifies energy management and transient coordination as essential design considerations alongside interruption speed, with experimental validation of the freewheeling path and further investigation of parallel switching remaining as future work.

Keywords: *Solid-state circuit breaker, AC protection, SiC, fault interruption, current limiting, MOV energy, parallel operation.*

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Με την ολοκλήρωση της παρούσας διπλωματικής εργασίας, θα ήθελα αρχικά να εκφράσω τις θερμές μου ευχαριστίες προς τον επιβλέποντα καθηγητή μου, Αντώνιο Αντωνόπουλο, και τον καθηγητή Βασίλειο Νικολαΐδη, για την καθοδήγηση, την εμπιστοσύνη και κυρίως για την εξαιρετική συνεργασία που είχαμε σε όλη τη διάρκεια της εκπόνησης της εργασίας. Η διαθεσιμότητά τους, οι ουσιαστικές παρατηρήσεις και οι συμβουλές τους συνέβαλαν καθοριστικά τόσο στην εξέλιξη της διπλωματικής όσο και στη δική μου επιστημονική προσέγγιση.

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Εκτεταμένη Ελληνική Περίληψη

1. Εισαγωγή, κίνητρο και στόχοι της εργασίας

Η προστασία των συστημάτων ηλεκτρικής ενέργειας στηρίζεται ιστορικά στους ηλεκτρομηχανικούς διακόπτες ισχύος, οι οποίοι συνδυάζουν απλή αρχή λειτουργίας, πολύ χαμηλές απώλειες αγωγής και υψηλή αξιοπιστία. Για περισσότερο από έναν αιώνα υπήρξαν ουσιαστικά ο μοναδικός πρακτικός τρόπος διακοπής ρευμάτων σφάλματος σε δίκτυα εναλλασσόμενου ρεύματος, σε κάθε στάθμη τάσης. Το ίδιο το σύστημα ηλεκτρικής ενέργειας, ωστόσο, μεταβάλλεται: η ηλεκτροκίνηση και η αυξανόμενη χρήση ηλεκτρικής ενέργειας σε βιομηχανικές και οικιακές εφαρμογές ενισχύονται, το ποσοστό του εξοπλισμού ηλεκτρονικών ισχύος μέσα στο δίκτυο αυξάνεται με επιταχυνόμενο ρυθμό, οι υποδομές ταχείας φόρτισης ηλεκτρικών οχημάτων εισέρχονται μαζικά στο δίκτυο διανομής, και η διεσπαρμένη παραγωγή από ανανεώσιμες πηγές έχει μετατρέψει την άλλοτε παθητική γραμμή διανομής σε ένα ενεργό σύστημα με αμφίδρομη ροή ισχύος.

Οι εξελίξεις αυτές επιβάλλουν νέες και αυστηρότερες απαιτήσεις στην αλυσίδα προστασίας. Οι μετατροπείς ηλεκτρονικών ισχύος εμφανίζουν πολύ περιορισμένη αντοχή σε βραχυκύκλωμα και απαιτούν χρόνους προστασίας της τάξης λίγων χιλιοστών του δευτερολέπτου ή και μικρότερους, ενώ η διεσπαρμένη παραγωγή μεταβάλλει το μέτρο, τη διεύθυνση και τη μορφή των ρευμάτων σφάλματος, δυσχεραίνοντας τον συντονισμό των συμβατικών σχημάτων προστασίας υπερέντασης.

Οι ηλεκτρομηχανικοί διακόπτες, παρά την ωριμότητά τους, δεν μπορούν να ικανοποιήσουν ταυτόχρονα όλες αυτές τις απαιτήσεις. Ο χρόνος διακοπής τους, τυπικά στην περιοχή 30–80 ms, είναι ασύμβατος με την προστασία ευαίσθητου εξοπλισμού ηλεκτρονικών ισχύος· οι μηχανικές επαφές τους φθείρονται και απαιτούν περιοδική συντήρηση· το τόξο που παράγουν περιορίζει τη χρήση τους σε κλειστά ή επικίνδυνα περιβάλλοντα. Οι περιορισμοί αυτοί έχουν στρέψει το ερευνητικό ενδιαφέρον προς ταχύτερες, ευέλικτες και "έξυπνες" διατάξεις προστασίας, με τον *διακόπτη ισχύος στερεάς κατάστασης* (Solid-State Circuit Breaker, SSCB) να αποτελεί σήμερα έναν από τους πλέον ενεργά ερευνώμενους υποψηφίους για εφαρμογές χαμηλής και μέσης τάσης.

Ο διακόπτης στερεάς κατάστασης αντικαθιστά τις κινούμενες επαφές με έναν ή περισσότερους ελεγχόμενους ημιαγωγικούς διακόπτες, όπως IGBT, IGCT, SiC MOSFET ή SiC JFET. Μπορεί να διακόψει το ρεύμα μέσα σε μικροδευτερόλεπτα, δεν έχει κινούμενα μέρη, δεν παράγει τόξο και μπορεί να λειτουργήσει εκατομμύρια φορές χωρίς σημαντική γήρανση των διακοπτικών στοιχείων. Το κύριο μειονέκτημά του είναι οι απώλειες αγωγής που συνδέονται με την πτώση τάσης των ημιαγωγών: ακόμη και με σύγχρονα στοιχεία, η πτώση αυτή είναι της τάξης των 1–3 V, γεγονός που μεταφράζεται σε σημαντικές συνεχείς απώλειες για ρεύματα εκατοντάδων ή χιλιάδων αμπέρ.

Στόχοι. Η εργασία μελετά τη χρήση διακοπτών στερεάς κατάστασης σε συστήματα εναλλασσόμενου ρεύματος, με έμφαση στα δίκτυα διανομής χαμηλής τάσης. Οι επιμέρους στόχοι είναι η δομημένη παρουσίαση των προκλήσεων προστασίας των σύγχρονων δικτύων, η ανασκόπηση και σύγκριση των τεχνολογιών διακοπής (ηλεκτρομηχανικής, υβριδικής,

συντονισμού και στερεάς κατάστασης) και των οικογενειών ημιαγωγικών στοιχείων ισχύος. Περιλαμβάνονται επίσης η ανάλυση της αρχιτεκτονικής και των τοπολογιών του διακόπτη στερεάς κατάστασης και η μελέτη της συμπεριφοράς τους σε μονοφασικά και τριφασικά συστήματα μέσω προσομοίωσης στο MATLAB/Simulink. Τέλος, πραγματοποιείται πειραματική επαλήθευση σε εμπορικά διαθέσιμη πλακέτα αξιολόγησης, με έλεγχο μέσω μικροεπεξεργαστή, και εξετάζονται η παράλληλη λειτουργία πολλαπλών μονάδων και ο χρόνος απόκρισης.

2. Σύγχρονα δίκτυα εναλλασσόμενου ρεύματος και προκλήσεις προστασίας

Η δομή των δικτύων διανομής χαμηλής και μέσης τάσης παρέμεινε επί δεκαετίες εξαιρετικά σταθερή: μονόδρομη ροή ισχύος, φορτία κυρίως γραμμικά, και προστασία βασισμένη κυρίως σε ηλεκτρονόμους υπερέντασης–χρόνου και ασφάλειες στη μέση τάση, και σε θερμομαγνητικούς μικροαυτόματους και ασφάλειες στη χαμηλή. Στο πλαίσιο αυτό, χρόνοι σβέσης τόξου αρκετών δεκάδων ms ήταν απολύτως αποδεκτοί.

Σήμερα η ίδια υποδομή καλείται να τροφοδοτήσει πολύ ευρύτερη ποικιλία φορτίων και να φιλοξενήσει αυξανόμενο αριθμό πηγών. Η σημαντικότερη μεμονωμένη αλλαγή είναι η επικράτηση των μετατροπέων ισχύος ως κύρια διεπαφή μεταξύ πηγών, φορτίων και δικτύου. Σε σύγκριση με τις περιστρεφόμενες μηχανές που σταδιακά αντικαθίστανται, οι μετατροπείς πηγής τάσης εμφανίζουν τρία χαρακτηριστικά καθοριστικά για τον σχεδιασμό της προστασίας. Πρώτον, έχουν πολύ μικρή ηλεκτρική αδράνεια: το ρεύμα εξόδου τους μεταβάλλεται πολύ ταχύτερα από τον δρομέα μιας σύγχρονης μηχανής, αλλά το μέγιστο ρεύμα που μπορούν να αποδώσουν περιορίζεται αυστηρά από το ονομαστικό ρεύμα των ημιαγωγών τους. Δεύτερον, η συμπεριφορά τους στα σφάλματα καθορίζεται κυρίως από τον αλγόριθμο ελέγχου και όχι μόνο από τις σύνθετες αντιστάσεις του κυκλώματος: τυπικές υλοποιήσεις περιορίζουν το ελεγχόμενο ρεύμα στο 1,1–1,5 του ονομαστικού. Ο έλεγχος μπορεί επίσης να περιορίζει επιλεκτικά συνιστώσες του ρεύματος, όπως τη συνιστώσα αρνητικής ακολουθίας σε ασύμμετρα σφάλματα, ανάλογα με τη στρατηγική ελέγχου. Αυτό δεν αποτελεί καθολική συμπεριφορά όλων των μετατροπέων [1]. Τρίτον, είναι εγγενώς ελεγχόμενοι, γεγονός που επιτρέπει προηγμένες λειτουργίες αλλά καθιστά το σύστημα πιο ευάλωτο στην απώλειά τους όταν τίθενται εκτός για αυτοπροστασία.

Η διεσπαρμένη παραγωγή από ανανεώσιμες πηγές αποτελεί την πιο ορατή έκφραση αυτής της μετάβασης. Σύμφωνα με τον Διεθνή Οργανισμό Ανανεώσιμων Πηγών Ενέργειας, η παγκόσμια εγκατεστημένη ισχύς ΑΠΕ υπερδιπλασιάστηκε τη δεκαετία 2015–2025, από 1.985 GW σε 5.149 GW, με τα φωτοβολταϊκά και τα αιολικά να καλύπτουν το μεγαλύτερο μέρος των νέων προσθηκών. Η ένταξή τους σε δίκτυα, που δεν σχεδιάστηκαν για αυτή την αύξηση, δημιουργεί ζητήματα αμφίδρομης ροής ισχύος, τοπικής ανύψωσης τάσης, αυξημένης αρμονικής παραμόρφωσης, μεταβολής των επιπέδων βραχυκύκλωσης για παράδειγμα με φαινόμενα "τύφλωσης" της προστασίας και απαιτήσεων αντι-νησιδοποίησης.

Στο ίδιο πλαίσιο εντάσσονται τα μικροδίκτυα και τα ενεργά δίκτυα διανομής, που απαιτούν ταυτόχρονη βελτίωση της επιλεκτικότητας, της ευαισθησίας και της ταχύτητας της προστασίας, υπό συνθήκες λειτουργίας συνεχώς μεταβαλλόμενες. Συνολικά, οι κύριες προκλήσεις προστασίας των σύγχρονων δικτύων εναλλασσόμενου ρεύματος συνοψίζονται

ως εξής: 1.ασυμβατότητα ταχύτητας προστασίας και ευαισθησίας φορτίων ,δηλαδή ο εξοπλισμός ηλεκτρονικών ισχύος αντέχει βραχυκύκλωμα μόνο για λίγα ms, ενώ ο ηλεκτρομηχανικός διακόπτης χρειάζεται δεκάδες ms, 2.αμφίδρομη ροή ισχύος, που επιβάλλει κατευθυντικά στοιχεία προστασίας και επανεξέταση του συντονισμού, 3.μεταβλητά και περιορισμένα από την πηγή επίπεδα σφάλματος, εξαρτώμενα από το πλήθος και τον τρόπο ελέγχου των συνδεδεμένων μετατροπέων, 4.διάκριση από ρεύματα εκκίνησης και μεταβατικά φορτίου (εκκίνηση κινητήρων, μαγνήτιση μετασχηματιστών, ζεύξη πυκνωτών, φόρτιση ηλεκτρικών οχημάτων), 5.απαιτήσεις ποιότητας ισχύος και συνέχειας τροφοδοσίας σε κέντρα δεδομένων και βιομηχανίες διεργασιών, 6.συμβατότητα με ψηφιακή προστασία και επικοινωνίες κατά IEC 61850.

Ανεξάρτητα από τη λογική της προστασίας, η πραγματική διακοπή του σφάλματος εξακολουθεί να εκτελείται από τον διακόπτη ισχύος, και η ταχύτητα και ελεγξιμότητά του καθορίζουν τελικά τι μπορεί ή δεν μπορεί να επιτύχει η προστασία.

3. Συμπεριφορά σφαλμάτων και απαιτήσεις προστασίας

Σε σύστημα εναλλασσόμενου ρεύματος τροφοδοτούμενο από σύγχρονες γεννήτριες ή από ισχυρό ανάντη δίκτυο, ένα βραχυκύκλωμα παράγει κυματομορφή ρεύματος με εναλλασσόμενη και, γενικά, μεταβατική συνεχή συνιστώσα, η οποία εξαρτάται από τη στιγμή εκδήλωσης του σφάλματος. Με το απλοποιημένο μοντέλο RL, το ρεύμα του βρόχου σφάλματος γράφεται

$$i(t) = \frac{V_m}{Z}\left[\sin(\omega t + \alpha - \varphi) - \sin(\alpha - \varphi)\, e^{-t\,R/L}\right],$$

όπου V_m είναι η μέγιστη τάση που τροφοδοτεί τον βρόχο σφάλματος, Z και φ το μέτρο και η γωνία της εμπέδησης του βρόχου, α η φασική γωνία της τάσης τη στιγμή του σφάλματος και L/R η σταθερά χρόνου του βρόχου. Ο πρώτος όρος αντιστοιχεί στη συμμετρική συνιστώσα μόνιμης κατάστασης και ο δεύτερος στη μεταβατική συνεχή μετατόπιση. Η στιγμιαία κορυφή του ρεύματος μπορεί επομένως να είναι πολύ υψηλότερη από την ενεργό τιμή μόνιμης κατάστασης, ιδίως όταν το σφάλμα εκδηλώνεται κοντά σε μηδενισμό της τάσης — συνθήκη που, για τις κατά κανόνα επαγωγικές εμπεδήσεις των κυκλωμάτων ισχύος, δίνει τη μέγιστη συνεχή μετατόπιση. Το κρίσιμο για την προστασία χαρακτηριστικό είναι ότι, μόλις αποσβεστεί η συνεχής μετατόπιση, το ρεύμα μηδενίζεται κάθε ημιπερίοδο: αυτή ακριβώς είναι η ιδιότητα που εκμεταλλεύονται επί έναν αιώνα οι μηχανικοί διακόπτες. Για σφάλματα με μεγάλη μετατόπιση και μεγάλη σταθερά χρόνου, ωστόσο, οι πρώτοι μηδενισμοί μπορεί να καθυστερήσουν αρκετές περιόδους.

Σε μια σύγχρονη γραμμή διανομής συνυπάρχουν πολλές πηγές ρεύματος σφάλματος: 1. το ανάντη δίκτυο, που συμπεριφέρεται ως πηγή τάσης Thévenin χαμηλής εμπέδησης και μπορεί να αποδώσει δεκάδες kA, 2.οι σύγχρονες μηχανές, των οποίων η συνεισφορά φθίνει από την υπομεταβατική τιμή με σταθερές χρόνου από δεκάδες ms έως δευτερόλεπτα, 3.οι μετατροπείς, των οποίων η συνεισφορά περιορίζεται στο 1,1–1,5 του ονομαστικού ρεύματος και εξαρτάται από τον τρόπο ελέγχου, 4.τα συστήματα αποθήκευσης, τα οποία μέσω των διόδων σώματος του αντιστροφέα τροφοδοτούν μεγάλα μεταβατικά ρεύματα ακόμη και όταν αυτός είναι εκτός, 5.οι πυκνωτές αντιστάθμισης, που αποδίδουν πολύ υψηλούς αλλά ακαριαίους παλμούς, επιβάλλοντας ακραία καταπόνηση $\mathrm{d}i/\mathrm{d}t$.

Από την ανάλυση αυτή προκύπτουν οι απαιτήσεις που θα έπρεπε ιδανικά να συνδυάζει ένα σύγχρονο σύστημα προστασίας: ταχεία λειτουργία (συνολικός χρόνος ανίχνευσης, απόφασης και διακοπής της τάξης λίγων ms ή μικρότερος), υψηλή ευαισθησία, αμφίδρομη ικανότητα διακοπής και απομόνωσης τάσης, επιλεκτικότητα και συντονισμός, διάκριση από μεταβατικά φαινόμενα, υψηλή αξιοπιστία και μεγάλη διάρκεια ζωής, χαμηλές απώλειες αγωγής του διακόπτη και συμβατότητα με ψηφιακή προστασία και επικοινωνίες. Καμία υπάρχουσα τεχνολογία δεν τις ικανοποιεί πλήρως και όλες ταυτόχρονα.

4. Τεχνολογίες διακοπτών ισχύος — ανασκόπηση

Ηλεκτρομηχανικοί διακόπτες. Βασίζονται σε ζεύγος μεταλλικών επαφών που διαχωρίζονται μηχανικά και σε ένα μέσο σβέσης του τόξου (αέρας, λάδι, SF_6 ή κενό) το οποίο εξασφαλίζει ότι, στον επόμενο φυσικό μηδενισμό του ρεύματος, το τόξο έχει περιοριστεί επαρκώς ώστε να μην επαναναφλεγεί υπό την τάση επανόδου. Πλεονεκτούν σε εξαιρετικά χαμηλές απώλειες αγωγής, κλιμάκωση σε οποιαδήποτε στάθμη τάσης, γαλβανική απομόνωση, ωριμότητα και χαμηλό κόστος. Ωστόσο, μειονεκτούν σε χρόνους λειτουργίας 30–80 ms, φθορά επαφών από το τόξο (τυπικά 10^3–10^4 χειρισμοί), ανάγκη συντήρησης και μειωμένη αποτελεσματικότητα όταν το ρεύμα δεν έχει σαφείς μηδενισμούς.

Υβριδικοί διακόπτες. Συνδυάζουν έναν ταχύ μηχανικό διακόπτη (τυπικά Thomson) σε σειρά με λίγους ημιαγωγούς, με έναν παράλληλο κλάδο μεταγωγής που φέρει τους κύριους ημιαγωγικούς διακόπτες και έναν τρίτο κλάδο απορρόφησης ενέργειας με βαρίστορ. Στην κανονική λειτουργία το ρεύμα ρέει σχεδόν αποκλειστικά από τον κλάδο χαμηλών απωλειών, που περιλαμβάνει τη μηχανική επαφή και τον βοηθητικό ημιαγωγικό διακόπτη. Κατά τη διακοπή μεταφέρεται στον παράλληλο κλάδο, ο μηχανικός διακόπτης ανοίγει χωρίς τόξο και οι ημιαγωγοί σβήνουν το ρεύμα, το οποίο οδηγείται τελικά στο βαρίστορ. Επιτυγχάνουν χρόνους λίγων ms με χαμηλές απώλειες, με τίμημα την αυξημένη πολυπλοκότητα και το κόστος.

Διακόπτες συντονισμού (εξαναγκασμένης μεταγωγής). Διατηρούν ως κύριο στοιχείο αγωγής ένα ημιελεγχόμενο θυρίστορ και προσθέτουν βοηθητικό κύκλωμα LC (προφορτισμένος πυκνωτής) που δημιουργεί κατά παραγγελία τεχνητό μηδενισμό του ρεύματος, ώστε το θυρίστορ να ανακτήσει την ικανότητα φραγής χωρίς αναμονή του φυσικού μηδενισμού. Κληρονομούν από το θυρίστορ πολύ χαμηλή πτώση τάσης αγωγής και εξαιρετική αντοχή σε κρουστικά ρεύματα, και πετυχαίνουν χρόνους διακοπής κάτω του χιλιοστού του δευτερολέπτου. Οι περιορισμοί τους είναι το βοηθητικό κύκλωμα μεταγωγής, ο χρόνος αντίδρασης που παραμένει μεγαλύτερος από αυτόν ενός τρανζίστορ, η εξάρτηση από τη σωστή πολικότητα προφόρτισης, και — κυρίως — η *απουσία δυνατότητας ενεργού περιορισμού ρεύματος*: η διακοπή είναι μια εφάπαξ, μη αναστρέψιμη ενέργεια που υπαγορεύεται από την ταλάντωση LC.

Διακόπτες στερεάς κατάστασης. Αντικαθιστούν πλήρως τις κινούμενες επαφές με ελεγχόμενους ημιαγωγικούς διακόπτες. Η σβέση του ημιαγωγού διαρκεί κλάσμα του μικροδευτερολέπτου, ενώ η πλήρης διακοπή, συμπεριλαμβανομένης της ανίχνευσης, της απόσυρσης της πύλης και του διαστήματος κατά το οποίο απομαγνητίζεται η επαγωγή του δικτύου, ολοκληρώνεται τυπικά σε μερικές δεκάδες έως λίγες εκατοντάδες μικροδευ-

τερόλεπτα. Τα πλεονεκτήματα είναι η υπερταχεία διακοπή χωρίς τόξο, η πλήρης ελεγξιμότητα (ο ίδιος διακόπτης λειτουργεί ταυτόχρονα ως διακόπτης προστασίας, περιοριστής ρεύματος και τηλεχειριζόμενος διακόπτης), η εξαιρετική διάρκεια ζωής ($> 10^6$ χειρισμοί), η απουσία κινούμενων μερών και θορύβου, ο συμπαγής όγκος, η συμβολή στην ευστάθεια και την ποιότητα ισχύος και η εγγενής δυνατότητα περιορισμού ρεύματος. Το τίμημα καταβάλλεται κυρίως σε απώλειες αγωγής.

Ο Πίνακας Π.1 συνοψίζει ποιοτικά τη σύγκριση των τεσσάρων οικογενειών.

Πίνακας Π.1. Ποιοτική σύγκριση των τεχνολογιών διακοπτών ισχύος.

Χαρακτηριστικό	**Ηλεκτρομηχανικός**	**Υβριδικός**	**Συντονισμού**	**Στερεάς κατάστασης**
Χρόνος διακοπής	30–80 ms	2–5 ms	0,1–1 ms	1–100 μs
Απώλειες αγωγής	Πολύ χαμηλές	Χαμηλές	Πολύ χαμηλές	Μέτριες–υψηλές
Δημιουργία τόξου	Ναι	Ελάχιστη	Όχι	Όχι
Διάρκεια ζωής (χειρ.)	10^3–10^4	10^4–10^5	$> 10^5$	$> 10^6$
Γαλβανική απομόνωση	Ναι	Ναι	Ναι	Απαιτεί βοηθ. διακόπτη
Συντήρηση	Περιοδική	Μειωμένη	Χαμηλή	Ελάχιστη
Σχετικό κόστος	Χαμηλό	Μέτριο–υψηλό	Μέτριο	Υψηλό
Δίκτυα με μετατροπείς	Περιορισμένη	Καλή	Καλή	Άριστη

5. Ημιαγωγικά στοιχεία ισχύος για διακόπτες στερεάς κατάστασης

Το ημιαγωγικό στοιχείο βρίσκεται στην καρδιά κάθε διακόπτη στερεάς κατάστασης: φέρει το ρεύμα φορτίου στη μόνιμη κατάσταση, το διακόπτει σε λίγα μικροδευτερόλεπτα και αντέχει την τάση επανόδου. Τα στοιχεία ταξινομούνται ως προς το υλικό (Si, SiC, GaN), τη φύση της μεταφοράς φορτίου (μονοπολικά ή διπολικά), την ελεγξιμότητα (μη ελεγχόμενα, ημιελεγχόμενα, πλήρως ελεγχόμενα), την πολικότητα αγωγής, και τη συμπεριφορά (normally ON, normally OFF).

Στοιχεία πυριτίου. Το *θυρίστορ* (SCR) προσφέρει εξαιρετική αντοχή σε κρουστικά ρεύματα, πολύ χαμηλή πτώση τάσης (1,0–1,5 V) και χαμηλό κόστος ανά αμπέρ, αλλά στερείται δυνατότητας σβέσης μέσω πύλης. Το *GTO* και η εξέλιξή του, το *ETO*, προσθέτουν πλήρη έλεγχο σε πολύ υψηλές τάσεις. Το *IGBT* αποτελεί το στοιχείο αναφοράς για μέση τάση και υψηλή ισχύ, χάρη στην απλή οδήγηση πύλης, τις χαμηλές απώλειες αγωγής και τον χρόνο αντοχής σε βραχυκύκλωμα 5–10 μs. Το *IGCT* και ιδίως η παραλλαγή του με αντίστροφη φραγή (RB-IGCT) συνδυάζουν πολύ χαμηλή πτώση τάσης σε μερικά kA με εγγενή αμφίδρομη φραγή, ιδιότητα ιδιαίτερα ελκυστική στα εναλλασσόμενα δίκτυα, όπου αποφεύγεται ο διπλασιασμός της πτώσης τάσης μιας αντι-σειριακής διάταξης. Το *MOSFET* ισχύος πυριτίου, τέλος, χαρακτηρίζεται από ωμική συμπεριφορά αγωγής και πολύ ταχεία μετάβαση, αλλά η $R_{DS(\mathrm{on})}$ αυξάνεται περίπου με την 2,4–2,5 δύναμη της τάσης διάσπασης, γεγονός που το καθιστά μη ανταγωνιστικό πάνω από τα 500–700 V.

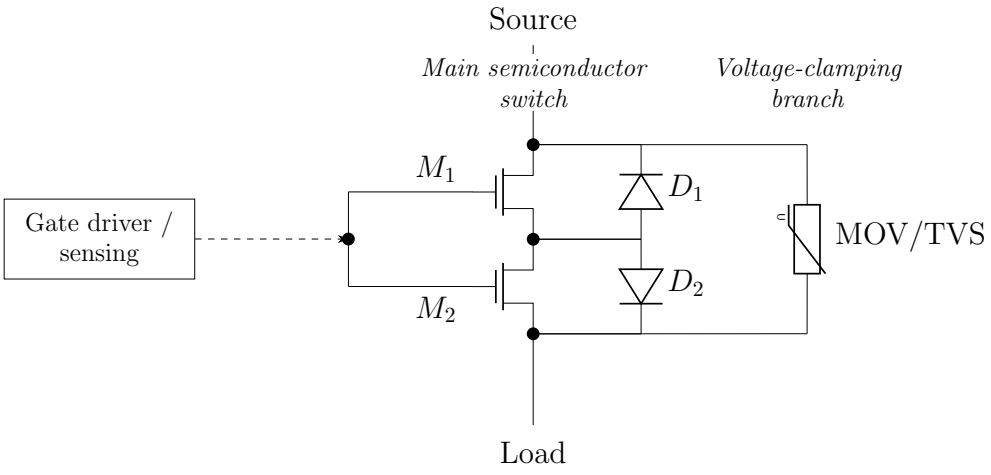
Στοιχεία ευρέος ενεργειακού διακένου. Το κρίσιμο ηλεκτρικό πεδίο του καρβιδίου του πυριτίου και του νιτριδίου του γαλλίου είναι περίπου δεκαπλάσιο εκείνου του πυριτίου, γεγονός που επιτρέπει λεπτότερες περιοχές ολίσθησης, χαμηλότερη αντίσταση αγωγής και ταχύτερη μετάβαση για δεδομένη τάση διάσπασης. Το *SiC MOSFET* είναι σήμερα το πιο ώριμο εμπορικά στοιχείο ευρέος διακένου (650 V έως 3,3 kV), με χρόνο σβέσης κάτω των 200 ns και θερμοκρασία λειτουργίας έως περίπου 200 °C. Περιορίζεται, όμως, από το κόστος, τον χρόνο αντοχής σε βραχυκύκλωμα μόλις 1–3 μs και ζητήματα αξιοπιστίας του οξειδίου πύλης. Το *SiC JFET* δεν διαθέτει οξείδιο πύλης, είναι εγγενώς ανθεκτικότερο και, στην normally ON εκδοχή του, άγει χωρίς καθόλου ισχύ οδήγησης της πύλης, ιδιότητα που αξιοποιείται σε αυτοτροφοδοτούμενες τοπολογίες διακοπτών. Πρέπει να τονιστεί ότι η έλξη του κανονικά αγώγιμου JFET εξασφαλίζει το μηδενικό κόστος αναμονής και τη δυνατότητα άντλησης της ενέργειας σβέσης από το ίδιο το σφάλμα. Συνεπώς, απαιτείται μηχανισμός ασφαλούς εκκίνησης, τυπικά με εν σειρά MOSFET χαμηλής τάσης σε διάταξη cascode ή άμεσης οδήγησης. Το *GaN HEMT* προσφέρει μεταβάσεις κάτω των 10 ns και τη δυνατότητα μονολιθικών αμφίδρομων διακοπτών, αλλά περιορίζεται σήμερα σε τάσεις έως 650 V και σε χρόνο αντοχής σε βραχυκύκλωμα μερικών εκατοντάδων ns. Τέλος, τα *διπολικά στοιχεία SiC* (SiC IGBT, SiC ETO, SiC GTO) έχουν δυνατότητα εφαρμογής σε 10–15 kV και αποτελούν τη μακροπρόθεσμη οδό προς αληθινούς διακόπτες μέσης και υψηλής τάσης.

Κριτήρια επιλογής. Η επιλογή προκύπτει από συμβιβασμό πολλαπλών κριτηρίων: ονομαστική τάση και ρεύμα, απώλειες αγωγής (τα διπολικά στοιχεία υπερέχουν σε υψηλά ρεύματα, τα μονοπολικά σε χαμηλά και μέτρια), διακοπτική ταχύτητα και ικανότητα σβέσης, χρόνος αντοχής σε βραχυκύκλωμα (που επιβάλλει ταχύτερη ανίχνευση όσο ταχύτερο γίνεται το στοιχείο), αμφίδρομη ικανότητα, πολυπλοκότητα και ισχύς οδήγησης πύλης, και κόστος. Για τους διακόπτες εναλλασσόμενου ρεύματος που στοχεύει η εργασία (230 V μονοφασικά και 400 V τριφασικά) η αντι-σειριακή διάταξη δύο SiC MOSFET αποτελεί τον πλέον ισορροπημένο συμβιβασμό, και αυτή υιοθετείται στις προσομοιώσεις. Η πειραματική διάταξη χρησιμοποιεί, αντ' αυτού, εμπορική πλακέτα με Combo JFET, στην οποία ένα κανονικά αγώγιμο SiC JFET τοποθετείται σε σειρά με MOSFET πυριτίου χαμηλής τάσης.

6. Αρχιτεκτονική, τοπολογίες και βοηθητικά κυκλώματα

Ο διακόπτης στερεάς κατάστασης περιγράφεται από τέσσερις λειτουργικές βαθμίδες: τον *κύριο ημιαγωγικό διακόπτη*, τον *κλάδο ψαλιδισμού τάσης και απορρόφησης ενέργειας* (τυπικά βαρίστορ οξειδίου μετάλλου, MOV), τον *οδηγητή πύλης* και το *σύστημα μέτρησης και ελέγχου*. Συχνά προστίθενται ένας εν σειρά μηχανικός απομονωτής (για γαλβανική απομόνωση, αφού πρώτα μηδενιστεί το ρεύμα), ένα πηνίο περιορισμού $\mathrm{d}i/\mathrm{d}t$ και ένα κύκλωμα απόσβεσης (snubber). Η ανάγκη για snubber εξαρτάται έντονα από την τεχνολογία: τα SCR και GTO συχνά χρειάζονται τέτοια κυκλώματα, ενώ στα IGCT το snubber σβέσης μπορεί να παραλειφθεί. Για IGBT είναι συχνά προαιρετικό, ενώ τα MOSFET ευρέος διακένου λειτουργούν συνήθως χωρίς snubber σβέσης.

Η σύνδεση των λειτουργικών βαθμίδων και του παράλληλου κλάδου απορρόφησης ενέργειας παρουσιάζεται στο Σχήμα Π.1.



Σχήμα Π.1. Γενική αρχιτεκτονική διακόπτη στερεάς κατάστασης: κύρια διαδρομή ισχύος, κλάδος απορρόφησης ενέργειας και σύστημα οδήγησης και ελέγχου.

Φάσεις της διακοπής. (1) Κανονική λειτουργία: ο διακόπτης άγει, η τάση επάνω του περιορίζεται στην πτώση αγωγής και το βαρίστορ βρίσκεται στην περιοχή διαρροής. (2) Ανίχνευση σφάλματος: το ρεύμα αποκλίνει από την ημιτονοειδή τροχιά του με ρυθμό $\mathrm{d}i/\mathrm{d}t = (v_s(t) - v_{\mathrm{arc}})/L$· επειδή η $v_s(t)$ είναι ημιτονοειδής, η απότομη ανάπτυξη εξαρτάται από το *σημείο του κύματος*. (3) Σβέση του κύριου διακόπτη: η σβέση επιβάλλεται ενεργά, χωρίς αναμονή φυσικού μηδενισμού, και ολοκληρώνεται σε λίγες εκατοντάδες ns έως λίγα μs. (4) Απορρόφηση ενέργειας: μόλις η τάση φτάσει τη στάθμη ψαλιδισμού, το ρεύμα εκτρέπεται στο βαρίστορ, το οποίο συμπεριφέρεται ως στοιχείο σχεδόν σταθερής τάσης. Η ενέργεια που απορροφά προσεγγίζεται από τη σχέση:

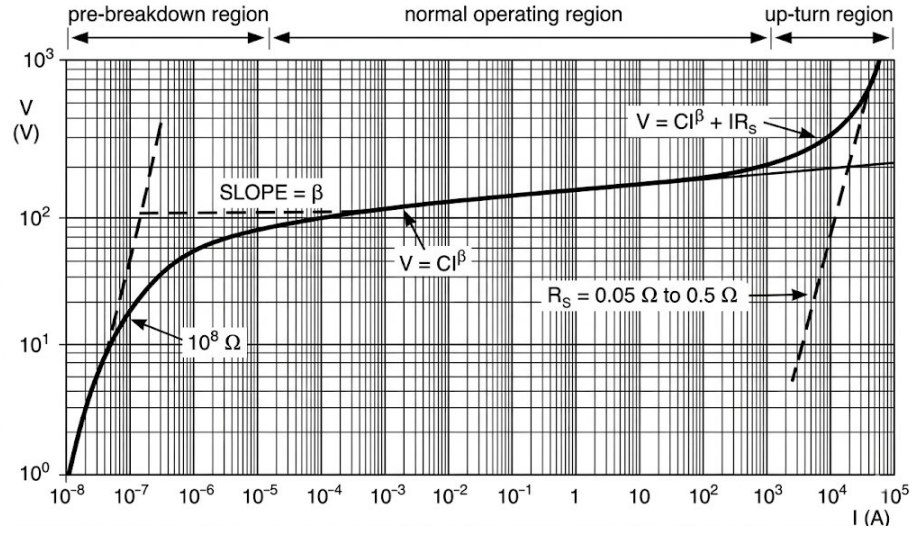
$$W_{\mathrm{MOV}} \approx \frac{1}{2}\, L\, I_{\mathrm{max}}^{2}\, \frac{V_{\mathrm{clamp}}}{V_{\mathrm{clamp}} - |v_s(t_0)|},$$

με μέγιστη ενέργεια κοντά στην κορυφή της τάσης πηγής για δεδομένο διακοπτόμενο ρεύμα. Επιπλέον περιορισμός, ειδικός για το εναλλασσόμενο ρεύμα, είναι ότι η τάση ψαλιδισμού πρέπει να βρίσκεται ασφαλώς πάνω από τη μέγιστη τάση του δικτύου ώστε το βαρίστορ να μην άγει σε κάθε ημιπερίοδο (τυπικός συμβιβασμός είναι $V_{\mathrm{clamp}} = (1{,}5\text{–}2{,}2)\,\hat{V}_s$). (5) Αποκατάσταση και απομόνωση: η τάση επανόδου στα άκρα του ανοιχτού διακόπτη είναι πλέον όλη η ημιτονοειδής τάση πηγής, την οποία πρέπει να αντέχουν τόσο ο ημιαγωγός όσο και το βαρίστορ.

Το βαρίστορ οξειδίου μετάλλου. Πρόκειται για κεραμικό όγκο από πυροσυσσωματωμένη σκόνη οξειδίου του ψευδαργύρου με πρόσθετα μεταλλικά οξείδια. Οι αγώγιμοι κόκκοι ZnO χωρίζονται από λεπτά μονωτικά στρώματα πάχους λίγων νανομέτρων, καθένα από τα οποία συμπεριφέρεται ως ζεύγος αντίθετα συνδεδεμένων ημιαγωγικών επαφών με τάση διάσπασης 3–3,5 V. Η διάταξη είναι επομένως ένα τρισδιάστατο δίκτυο σειράς και παραλληλίας τέτοιων μικροσκοπικών επαφών: το πάχος του κεραμικού καθορίζει την τάση του βαρίστορ και η επιφάνεια των ηλεκτροδίων την ικανότητα ρεύματος και ενέργειας. Η χαρακτηριστική τάσης–ρεύματος περιγράφεται από τον εμπειρικό νόμο δύναμης $I = k\,V^{\alpha}$, με τον συντελεστή μη γραμμικότητας α στην περιοχή 25–50 για ZnO. Ισοδύναμα, οι κατα-

σκευαστές παραθέτουν τον αντίστροφο εκθέτη $\beta = 1/\alpha \approx 0{,}03$–$0{,}05$ στη μορφή $V = C\,I^{\beta}$. Με $\alpha = 30$, μεταβολή του ρεύματος κατά τρεις τάξεις μεγέθους μεταβάλλει την τάση μόλις κατά 26 %. Ακριβώς αυτή η σχεδόν ανεξαρτησία δικαιολογεί την προσέγγιση σταθερής τάσης. Διακρίνονται τρεις περιοχές: η περιοχή διαρροής (όπου βρίσκεται το βαρίστορ ενός διακόπτη στην κανονική λειτουργία), η περιοχή ψαλιδισμού (το χρήσιμο σχεδόν οριζόντιο μέρος) και η περιοχή ανόδου σε πολύ υψηλά ρεύματα, όπου η ωμική αντίσταση των κόκκων δεν είναι πλέον αμελητέα. Ένα ζήτημα για την εφαρμογή του διακόπτη είναι ότι το βαρίστορ καταπονείται κοντά στην περιοχή ψαλιδισμού του σε κάθε διακοπή, με αποτέλεσμα τη σταδιακή γήρανση των φραγμών ανάμεσα στους κόκκους.

Στο Σχήμα Π.2 διακρίνονται οι περιοχές της χαρακτηριστικής του βαρίστορ, με χρήσιμη για τη διακοπή την περιοχή ψαλιδισμού τάσης.



Σχήμα Π.2. Χαρακτηριστική τάσης-ρεύματος του βαρίστορ οξειδίου μετάλλου και περιοχές λειτουργίας του.

Τοπολογίες εναλλασσόμενου ρεύματος. Η αντι-σειριακή (back-to-back) διάταξη δύο μονοκατευθυντικών διακοπτών με αντίθετα προσανατολισμένες διόδους είναι η απλούστερη και πιο διαδεδομένη στη χαμηλή τάση, υστερεί όμως στη διπλή πτώση τάσης αγωγής. Οι διατάξεις κοινής πηγής (Common Source) για MOSFET και κοινού εκπομπού (Common Emitter) για IGBT απλοποιούν την οδήγηση, καθώς οι δύο πύλες έχουν κοινό δυναμικό αναφοράς. Τα στοιχεία αντίστροφης φραγής (RB-IGBT, RB-IGCT) προσφέρουν κομψότερη λύση με μειωμένο πλήθος στοιχείων. Η τοπολογία γέφυρας διόδων με έναν διακόπτη απαιτεί έναν μόνο κύριο διακόπτη και έναν οδηγητή (Driver), αλλά επιβάλλει τρεις διαδοχικές πτώσεις τάσης. Η επιβάρυνση των απωλειών αγωγής εξαρτάται από τα στοιχεία, το ρεύμα και τη θερμοκρασία [2]. Οι διατάξεις με αντιπαράλληλα SCR αξιοποιούν την υψηλή αντοχή σε κρουστικά ρεύματα και το χαμηλό κόστος, αλλά απαιτούν εξαναγκασμένη σβέση. Οι συγγενείς οικογένειες Z-source και T-source έχουν μελετηθεί κυρίως για συνεχές ρεύμα και χρειάζονται κατάλληλη προσαρμογή για εναλλασσόμενο. Για τριφασικά συστήματα, η απλούστερη υλοποίηση είναι ένας αμφίδρομος διακόπτης ανά φάση με συντονισμένο έλεγχο.

Ανίχνευση σφάλματος. Χρησιμοποιούνται η ανίχνευση υπερέντασης με κατώφλι (τυπικά

2–3 φορές το ονομαστικό ρεύμα), η ανίχνευση κλίσης $\mathrm{d}i/\mathrm{d}t$ (ταχύτερη, αλλά με μεγαλύτερο κίνδυνο εσφαλμένης λειτουργίας) και η μέτρηση της τάσης απαγωγού–πηγής έναντι κατωφλίου, με αισθητήρες τύπου shunt, πηνία Rogowski, φαινομένου Hall ή GMR.

Εφαρμογές. Βιομηχανική διανομή και προστασία κινητήρων, κέντρα δεδομένων και κρίσιμα φορτία, οικιακή και εμπορική διανομή, υποδομές φόρτισης ηλεκτρικών οχημάτων, σταθμοί ΑΠΕ, μικροδίκτυα, ναυτιλιακά και αεροδιαστημικά συστήματα, σιδηροδρομική έλξη και εφαρμογές παλμικής ισχύος. Ιδιαίτερη σημασία, για δίκτυα με υψηλή διείσδυση ΑΠΕ, έχει η δυνατότητα περιορισμού του πραγματικού ρεύματος σφάλματος και της διάρκειάς του. Ο διακόπτης στερεάς κατάστασης μπορεί να αποκόψει έγκαιρα τη συνεισφορά μιας πηγής ή να περιορίσει προσωρινά το ρεύμα της. Η πιθανή αύξηση του περιθωρίου σύνδεσης παραγωγής απαιτεί μελέτη της αντοχής του εξοπλισμού και του συντονισμού των προστασιών, με σεβασμό στις εφαρμοστέες απαιτήσεις LVRT [3]. Δεν συνεπάγεται αυτόματη μείωση της δυνητικής στάθμης βραχυκύκλωσης του δικτύου χωρίς τη διάταξη περιορισμού.

7. Μοντελοποίηση και αποτελέσματα προσομοίωσης

7.1 Μονοφασικό σύστημα

Το μονοφασικό κύκλωμα δοκιμής αποτελείται από ημιτονοειδή πηγή 230 V (ενεργός τιμή), 50 Hz, η οποία τροφοδοτεί εν σειρά ωμικό–επαγωγικό φορτίο ($R = 4{,}6\,\Omega$, $L = 10\,\mathrm{mH}$) μέσω του διακόπτη· η γραμμή μοντελοποιείται με $0{,}01\,\Omega$ και $0{,}5\,\mathrm{mH}$. Το σφάλμα εφαρμόζεται παράλληλα στο φορτίο τη στιγμή $t = 0{,}1\,\mathrm{s}$. Η μέγιστη τιμή του ρεύματος μόνιμης κατάστασης είναι περίπου 58 A, αρκετά κάτω από το κατώφλι ανίχνευσης των 100 A. Η βαθμίδα ισχύος υλοποιείται ως αντι-σειριακό ζεύγος SiC MOSFET (ST SCTWA90N65G2V, $R_{ds(\mathrm{on})} = 17\,\mathrm{m}\Omega$) με το θερμικό μοντέλο του κατασκευαστή, ώστε οι απώλειες αγωγής και μεταγωγής και η θερμοκρασία επαφής να υπολογίζονται με ακρίβεια και συνέπεια. Το βαρίστορ ψαλιδίζει στα 480 V, δηλαδή περίπου 1,5 φορές τη μέγιστη τάση πηγής.

Η λογική ελέγχου περιλαμβάνει τρεις βαθμίδες. Η αναγνώριση σφάλματος συγκρίνει την απόλυτη τιμή του ρεύματος με το κατώφλι των 100 A και θέτει μανδαλωτή SR, ώστε ο διακόπτης να μην επανακλείνει αυτόματα. Ο περιοριστής ρεύματος διατηρεί το ρεύμα εντός ζώνης υστέρησης, διακόπτοντας και επαναφέροντας την πύλη. Κρίσιμη σχεδιαστική επιλογή είναι ότι η παράμετρος που ορίζεται δεν είναι το εύρος της ζώνης αλλά ο ελάχιστος χρόνος παραμονής $t_{\min}$ σε κάθε κατάσταση, ο οποίος θέτει σαφές άνω φράγμα στη διακοπτική συχνότητα, $f_{sw,\max} = 1/(2\,t_{\min})$· με $t_{\min} = 0{,}2\,\mathrm{ms}$ προκύπτει $f_{sw,\max} = 2{,}5\,\mathrm{kHz}$, ώστε οι απώλειες μεταγωγής και η διακοπτική συχνότητα να περιορίζονται ανεξάρτητα από τις παραμέτρους του κυκλώματος. Η διάρκεια του παραθύρου περιορισμού (0,035 s) ορίζεται από χωριστό μετρητή χρόνου, μετά τον οποίο ο διακόπτης εκτελεί οριστική διακοπή στον πρώτο φυσικό μηδενισμό του ρεύματος, επιλογή που εξασφαλίζει ότι η παγιδευμένη μαγνητική ενέργεια $\frac{1}{2}Li^2$ είναι ουσιαστικά μηδενική τη στιγμή της διακοπής. Τέλος, η *θερμική προστασία* επιβάλλει σβέση αν η θερμοκρασία επαφής υπερβεί τους 120 °C, ενώ η συνολική εντολή περνά από σταθερή καθυστέρηση διάδοσης 20 μs που συμβολίζει τον χρόνο εντοπισμού του σφάλματος.

Περίπτωση 1 — άμεση διακοπή. Μόλις το ρεύμα φτάσει τα 100 A, ο διακόπτης ενερ-

γοποιείται και το ρεύμα μηδενίζεται σε λιγότερο από ένα χιλιοστό του δευτερολέπτου. Η τάση φορτίου καταρρέει ταυτόχρονα, επιβεβαιώνοντας την απομόνωση του σφάλματος, και η θερμοκρασία επαφής φθίνει εκθετικά.

Περίπτωση 2 — διακοπή με περιορισμό ρεύματος. Το ρεύμα συγκρατείται εντός της ζώνης για 0,04 s πριν την οριστική διακοπή. Το όφελος είναι ο ελεγχόμενος περιορισμός χωρίς απότομη διακοπή, που μειώνει τα μεταβατικά τάσης και δίνει χρόνο συντονισμού σε ανάντη και κατάντη διατάξεις· το κόστος είναι ότι ο διακόπτης εξακολουθεί να άγει και επομένως να θερμαίνεται σε αυτό το χρονικό παράθυρο.

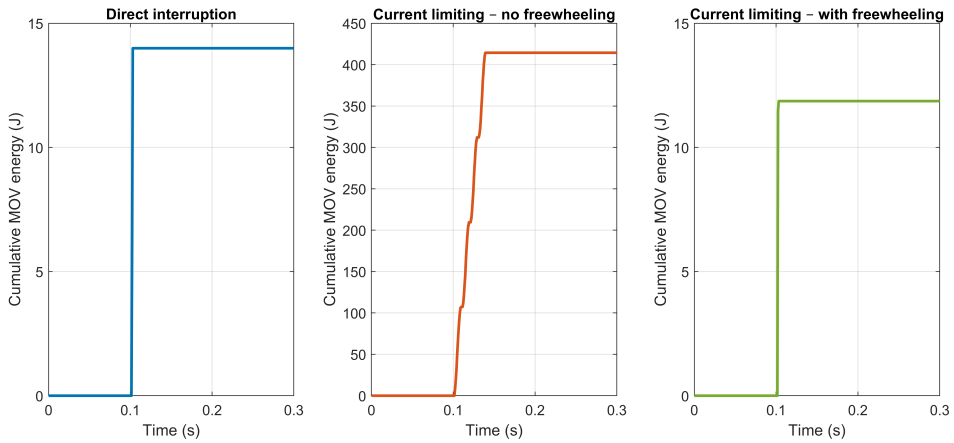
Επίδραση της διακοπτικής συχνότητας. Η μελέτη επαναλήφθηκε για 1, 2,5 και 5 kHz (Πίνακας Π.2). Η συχνότητα ελέγχει κυρίως το πόσο πιστά περιορίζεται το ρεύμα στη ζώνη: με μεγάλο $t_{\min}$ το ρεύμα προλαβαίνει να ξεφύγει σημαντικά πριν διορθωθεί. Αντίθετα, η θερμοκρασία επαφής παραμένει σχεδόν αμετάβλητη και στις τρεις περιπτώσεις, περίπου στην τιμή μόνιμης κατάστασης πριν το σφάλμα. Το αποτέλεσμα αυτό είναι το αναμενόμενο: ο ελεγκτής υστέρησης σχεδιάζεται ώστε να διατηρεί το ρεύμα κοντά στην ενεργό τιμή κανονικής λειτουργίας, οπότε η μέση ισχύς που εκλύεται είναι συγκρίσιμη με εκείνη της κανονικής λειτουργίας. Ωστόσο πρέπει να τονιστεί ότι αυτή η θερμική συμπεριφορά είναι ειδική για το συγκεκριμένο μοντέλο απωλειών και τις παραμέτρους του δικτύου.

Πίνακας Π.2. Επίδραση της μέγιστης διακοπτικής συχνότητας του περιοριστή στο ρεύμα γραμμής και στη θερμοκρασία επαφής.

Μέγιστη διακοπτική συχνότητα	**Ελάχιστος χρόνος παραμονής**	**Κορυφή $\lvert i_{\text{line}}\rvert$**	**T_j στο παράθυρο περιορισμού**
1 kHz	0,5 ms	≈ 130 A	≈ 85–90 °C
2,5 kHz	0,2 ms	≈ 90 A	≈ 80–85 °C
5 kHz	0,1 ms	≈ 65 A	≈ 82–85 °C

Διαχείριση της ενέργειας του βαρίστορ. Η στρατηγική περιορισμού, αν και αβλαβής για τους ημιαγωγούς, είναι καταστροφική για το βαρίστορ αν αυτό αφεθεί να ψαλιδίζει κάθε μία από τις πολλές σβέσεις μέσα στο παράθυρο. Η λύση που υιοθετείται είναι μια ελεγχόμενη διαδρομή ελεύθερης εκφόρτισης: μια γέφυρα διόδων γύρω από το αντι-σειριακό ζεύγος ανορθώνει το ρεύμα γραμμής σε ζυγό συνεχούς, στα άκρα του οποίου συνδέονται εν σειρά ένας ελεγχόμενος διακόπτης και μια αντίσταση απορρόφησης R_{dump}. Σε κάθε σβέση το ρεύμα μεταπίπτει σε αυτή τη διαδρομή και φθίνει με σταθερά χρόνου $\tau = L/R_{\text{dump}}$, αντί να διέλθει από το βαρίστορ. Η επιλογή ανόρθωσης, αντί ενός αμφίδρομου κυκλώματος βραχυκύκλωσης απευθείας στην πλευρά εναλλασσομένου, δικαιολογείται γιατί ο ζυγός συνεχούς έχει σταθερή πολικότητα και μπορεί να ελεγχθεί από *ένα* μόνο στοιχείο με μη απομονωμένη οδήγηση πύλης (Gate Drive), ενώ οι τέσσερις δίοδοι είναι παθητικές, φθηνές και ανθεκτικές. Ποσοτικά, για την περίπτωση των 2,5 kHz: χωρίς τη διαδρομή, η ενέργεια του βαρίστορ συσσωρεύεται κλιμακωτά και φτάνει περίπου τα 450 J στα 40 ms, δηλαδή τριάντα φορές πάνω από τα 14 J μιας άμεσης διακοπής ενώ με τη νέα διαδρομή ενεργή, μειώνεται σε περίπου 12 J (συγκρίσιμη με μία μόνο άμεση διακοπή).

Το Σχήμα Π.3 δείχνει ότι μικρότερο ρεύμα κατά τον περιορισμό δεν σημαίνει μικρότερη συνολική ενέργεια στο βαρίστορ.



Σχήμα Π.3. Ενέργεια που απορροφά το βαρίστορ στη μονοφασική προσομοίωση: άμεση αποκοπή, περιορισμός ρεύματος χωρίς πρόσθετη διαδρομή και περιορισμός με ελεγχόμενη διαδρομή εκφόρτισης.

Σύγκριση με διακόπτη συντονισμού και ηλεκτρομηχανικό. Το ίδιο σφάλμα εφαρμόστηκε στο ίδιο δίκτυο υπό τέσσερις συνθήκες (Πίνακας Π.3). Χωρίς διακόπτη, το ρεύμα εξελίσσεται σε βραδέως αποσβεννύμενη ταλάντωση με πρώτη κορυφή περίπου 1260 A. Ο ηλεκτρομηχανικός διακόπτης ακολουθεί *ακριβώς την ίδια* τροχιά — μέχρι να χωριστούν οι επαφές του είναι απλώς ένας κλειστός διακόπτης — και διαφοροποιείται μόνο στο ότι το ρεύμα μηδενίζεται τελικά σε φυσικό μηδενισμό γύρω στα $t = 0{,}137\,\mathrm{s}$. Η μηχανική του καθυστέρηση δεν προσφέρει τίποτε ως προς την κορυφή. Ο διακόπτης συντονισμού αποδίδει σημαντικά καλύτερα, διακόπτοντας περίπου στα 680 A. Ο διακόπτης στερεάς κατάστασης ανήκει σε άλλη κατηγορία: διακόπτει μόλις το ρεύμα περάσει το κατώφλι ανίχνευσης, κρατώντας το διερχόμενο ρεύμα οριακά πάνω από αυτό. Η διαφορά στη διερχόμενη ενέργεια $\int i^2 \mathrm{d}t$ (το μέγεθος που καθορίζει τη θερμική και μηχανική καταπόνηση) είναι πολύ μεγαλύτερη από όσο θα υποδήλωνε η διαφορά κορυφής, καθώς ο ηλεκτρομηχανικός διακόπτης επιτρέπει στο πλήρες ρεύμα να περάσει για δύο ημιπεριόδους.

Πίνακας Π.3. Χρόνος διακοπής και μέγιστο διερχόμενο ρεύμα για τις τρεις τεχνολογίες.

Τεχνολογία διακοπής	**Χρόνος διακοπής**	**Μέγιστο διερχόμενο ρεύμα**
Χωρίς διακόπτη	δεν διακόπτεται	1260 A (πρώτη κορυφή)
Ηλεκτρομηχανικός	36 ms	1260 A
Συντονισμού (LC)	5 ms	680 A
Στερεάς κατάστασης	0,8 ms	100 A

7.2 Τριφασικό δίκτυο διανομής

Η ανάλυση επεκτάθηκε σε υποδειγματική τριφασική ακτινική γραμμή μέσης τάσης, η οποία βασίζεται σε τυπικά δεδομένα του ελληνικού δικτύου των 20 kV [4]. Η γραμμή

είναι ανομοιογενής: ο κύριος κορμός δομείται από εναέριες γραμμές φθίνουσας διατομής με την απόσταση από τον υποσταθμό, ενώ οι διακλαδώσεις χρησιμοποιούν την μικρότερη διατομή. Το ανάντη δίκτυο των 150 kV παριστάνεται με ισχύ βραχυκύκλωσης 250 MVA και λόγο $X/R = 7$, και τροφοδοτεί τη γραμμή μέσω μετασχηματιστή 40 MVA, 150/20 kV. Ο κορμός χωρίζεται σε τέσσερα τμήματα των 5 km και οι τέσσερις διακλαδώσεις έχουν μήκος 3 km, με φορτία $R = 415\,\Omega$ και $L = 0{,}779$ H ανά φάση.

Η τοπική μονάδα διεσπαρμένης παραγωγής είναι σύγχρονη γεννήτρια κυλινδρικού δρομέα 5 MVA, 800 V, με σταθερά αδράνειας $H = 3{,}525$ s, συνδεδεμένη μέσω μετασχηματιστή ανύψωσης 5,2 MVA, 0,8/20 kV, και παράγει 3 MW πριν το σφάλμα. Είναι εξοπλισμένη με αυτόματο ρυθμιστή τάσης τύπου IEEE AC1C (κέρδος $K_A = 300$) και ρυθμιστή στροφών με στατισμό 4 %. Το στερεό τριφασικό βραχυκύκλωμα προς γη εφαρμόζεται στα $t = 3{,}8$ s. Η χρονική στιγμή επιλέγεται ώστε η γεννήτρια και οι ρυθμιστές της να έχουν ισορροπήσει στο προ σφάλματος σημείο λειτουργίας, μετά την απόσβεση των ηλεκτρομαγνητικών και ηλεκτρομηχανικών μεταβατικών της αρχικοποίησης του μοντέλου.

Εξετάζονται δύο θέσεις εγκατάστασης. Η θέση *στην αρχή της γραμμής*, αμέσως μετά τον μετασχηματιστή 150/20 kV, απαιτεί ηλεκτρονικά ισχύος ικανά να λειτουργούν σε 20 kV. Δεδομένου ότι τα εμπορικά SiC MOSFET φτάνουν σήμερα περίπου τα 3,3 kV, αυτό απαιτεί σειριακή σύνδεση πολλών στοιχείων και παραμένει μια θεωρητική περίπτωση.

Διαμόρφωση με παθητικά φορτία. Το τριφασικό αποτέλεσμα επιβεβαιώνει ότι ο διακόπτης και η λογική ελέγχου του λειτουργούν σωστά όταν επεκταθούν στις τρεις φάσεις. Το φαινόμενο που είναι γνήσια τριφασικό, και έχει άμεση επίπτωση στη διαστασιολόγηση, είναι η άνιση καταπόνηση των τριών βαριστόρ. Αν και οι τρεις πόλοι λαμβάνουν κοινή εντολή και ανοίγουν ταυτόχρονα, τα τρία ρεύματα απέχουν 120°, οπότε κάθε πόλος διακόπτει διαφορετική στιγμιαία τιμή. Οι συνέπειες είναι τρεις: 1.η πολικότητα της αιχμής ψαλιδισμού ακολουθεί το πρόσημο του ρεύματος, 2.η διάρκεια απόσβεσης του ρεύματος κάθε MOV διαφέρει, καθώς εξαρτάται από τη στιγμιαία τιμή του ρεύματος κατά την αποκοπή και την επαγωγή του βρόχου, 3. η ενέργεια $W = \int v_{\mathrm{MOV}}\, i_{\mathrm{MOV}}\, \mathrm{d}t$ είναι μεγαλύτερη στη φάση που τυχαίνει να διακόπτει κοντά στην κορυφή του. Επειδή το σημείο του κύματος δεν ελέγχεται από τον σχεδιαστή, κάθε βαρίστορ πρέπει να διαστασιολογείται για τη χειρότερη μονοφασική ενέργεια και όχι για τη μέση τιμή των τριών. Στο μοντέλο, η στάθμη ψαλιδισμού ορίστηκε στα 21 kV ανά πόλο, περίπου 1,3 φορές τη μέγιστη φασική τάση ως προς γη, ενώ η τάση επανόδου μετά τη διακοπή είναι ημιτονοειδής πλάτους περίπου 16,3 kV.

Διαμόρφωση με τοπική σύγχρονη γεννήτρια. Πρόκειται για την κεντρική περίπτωση του κεφαλαίου, καθώς αποκαλύπτει την αλληλεπίδραση μεταξύ της ταχύτητας διακοπής και της ηλεκτρομηχανικής δυναμικής μιας απευθείας συνδεδεμένης μηχανής. Ο διακόπτης τοποθετείται στην πλευρά των 800 V και προστατεύει τον κλάδο της γεννήτριας, ενώ το σφάλμα εφαρμόζεται στον ζυγό B_3 του κορμού. Ο ρόλος του είναι επομένως να απομονώσει και να προστατεύσει τη γεννήτρια, όχι να σβήσει το σφάλμα του κορμού.

Με τον διακόπτη στερεάς κατάστασης το ρεύμα στάτη μηδενίζεται μέσα σε λίγα ms, πριν προλάβουν να αναπτυχθούν οι ηλεκτρομηχανικές δυναμικές. Με τον ηλεκτρομηχανικό διακόπτη, αντίθετα, το ρεύμα φτάνει περίπου 3,75 p.u. (έξι φορές πάνω από την προ σφάλματος τιμή) και διατηρείται για περίπου 40 ms. Αμέσως μετά τη διακοπή από

τον διακόπτη στερεάς κατάστασης, η τάση ακροδεκτών ανεβαίνει στιγμιαία στα 1,9 p.u.: πρόκειται για την τάση επανόδου στον ανοιχτό πόλο, καθώς ο ρυθμιστής τάσης, που είχε αρχίσει να ανεβάζει την τάση διέγερσης, βρίσκεται πλέον να ρυθμίζει μηχανή χωρίς φορτίο.

Η σύγκριση των εσωτερικών μεγεθών της μηχανής είναι σημαντική. Η τάση διέγερσης E_{fd} φτάνει περίπου 2,7 φορές την αρχική της τιμή με τον ηλεκτρομηχανικό διακόπτη, ενώ με τον διακόπτη στερεάς κατάστασης η απόκλιση είναι αμελητέα. Η ηλεκτρική ροπή ταλαντώνεται μεταξύ περίπου $-0{,}5$ και $+2{,}5$ p.u. με τον ηλεκτρομηχανικό διακόπτη, επιβάλλοντας σημαντική κυκλική μηχανική καταπόνηση στον άξονα ενώ με τον διακόπτη στερεάς κατάστασης πέφτει καθαρά στο μηδέν μέσα σε μικροδευτερόλεπτα. Τέλος, η απόκλιση ταχύτητας του δρομέα (μικρή και στις δύο περιπτώσεις λόγω της μεγάλης αδράνειας) εμφανίζει χαρακτηριστική ταλάντωση με τον ηλεκτρομηχανικό, ενώ με τον διακόπτη στερεάς κατάστασης παρατηρείται μόνο μονότονη, αργή επιτάχυνση λόγω της απώλειας ηλεκτρικού φορτίου. Το αποτέλεσμα δείχνει, σε επίπεδο μονάδας, περιορισμό της διάρκειας συνεισφοράς της γεννήτριας στο σφάλμα. Η αξιοποίηση αυτής της δυνατότητας για αύξηση της διείσδυσης διεσπαρμένης παραγωγής προϋποθέτει μελέτη συντονισμού, έλεγχο της καταπόνησης του εξοπλισμού και συμβατότητα με τις εφαρμοστέες απαιτήσεις LVRT.

8. Πειραματική επαλήθευση

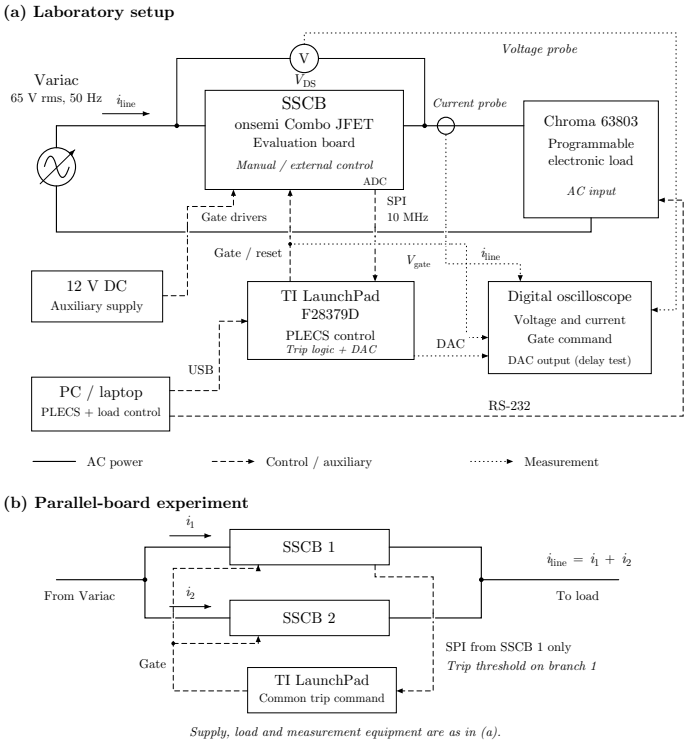
8.1 Πειραματική διάταξη

Η υπό δοκιμή διάταξη είναι η πλακέτα αξιολόγησης onsemi Combo JFET SSCB (EVBUM-2926/D), δομημένη γύρω από το στοιχείο UG4SC075005L8S σε περίβλημα TOLL. Το Combo JFET είναι σύνθετο στοιχείο που ενσωματώνει MOSFET πυριτίου χαμηλής τάσης σε σειρά με κανονικά αγώγιμο SiC JFET υψηλής τάσης. Σε αντίθεση με τη συμβατική διάταξη cascode, όπου η πύλη του JFET συνδέεται μόνιμα στην πηγή του MOSFET, το Combo JFET εξάγει και τις δύο πύλες ως ανεξάρτητους ακροδέκτες. Ο επιπλέον αυτός βαθμός ελευθερίας αξιοποιείται για μείωση της αντίστασης αγωγής, για ανεξάρτητο έλεγχο της ταχύτητας μετάβασης και για έμμεση εκτίμηση της θερμοκρασίας επαφής μέσω της τάσης πύλης–πηγής (V_{GS}), ενώ το στοιχείο διατηρεί συνολικά κανονικά μη αγώγιμη συμπεριφορά.

Η βαθμίδα ισχύος είναι αμφίδρομη, δομημένη από τέσσερις όμοιες κυψέλες (δύο JFET παράλληλα ανά πολικότητα, σε σειριακή διάταξη κοινής πηγής), με κυκλώματα απόσβεσης RC, δίοδο TVS και βαρίστορ για την ενέργεια των παρασιτικών επαγωγών. Το ρεύμα μετράται με αντιστάσεις shunt, ενώ συγκριτής υπερέντασης υλικού μανδαλώνει τον διακόπτη στην κατάσταση σβέσης. Η πλακέτα δέχεται 0–350 V με συνεχές ονομαστικό ρεύμα $10\,\mathrm{A_{rms}}$. Η πλακέτα συνδέθηκε σε προγραμματιζόμενο ηλεκτρονικό φορτίο Chroma 63803, ενώ η τροφοδοσία προερχόταν από μεταβλητό αυτομετασχηματιστή στα $55-65\,\mathrm{V_{rms}}$.

Για τις δοκιμές με εξωτερικό έλεγχο χρησιμοποιήθηκε η πλακέτα Texas Instruments LaunchPad F28379D. Η λογική υλοποιήθηκε σε μοντέλο PLECS. Το ρεύμα γραμμής δεν διαβάζεται από τον ενσωματωμένο μετατροπέα του επεξεργαστή αλλά από τον μετατροπέα 16 bit της πλακέτας onsemi, μέσω ζεύξης SPI στα 10 MHz. Κάθε μετατροπή φτάνει ως τρεις διαδοχικές λέξεις των 8 bit που ανασυντίθενται με βάρη 2^{12}, 2^{4} και 2^{-4}. Ακολουθεί μετατροπή σε φυσικές μονάδες (κλίμακα $3{,}3\,\mathrm{V}/2^{20}$, αφαίρεση της πόλωσης μηδενικού ρεύματος 1,576 V και ευαισθησία 74,12 A/V).

Η ροή ισχύος και οι συνδέσεις μέτρησης και ελέγχου συνοψίζονται στο Σχήμα Π.4, τόσο για μία μονάδα όσο και για δύο μονάδες σε παράλληλη λειτουργία.



Σχήμα Π.4. Σχηματική πειραματική διάταξη για μία μονάδα και για δύο παράλληλες μονάδες, με μεταβλητό αυτομετασχηματιστή, ηλεκτρονικό φορτίο και εξωτερικό έλεγχο.

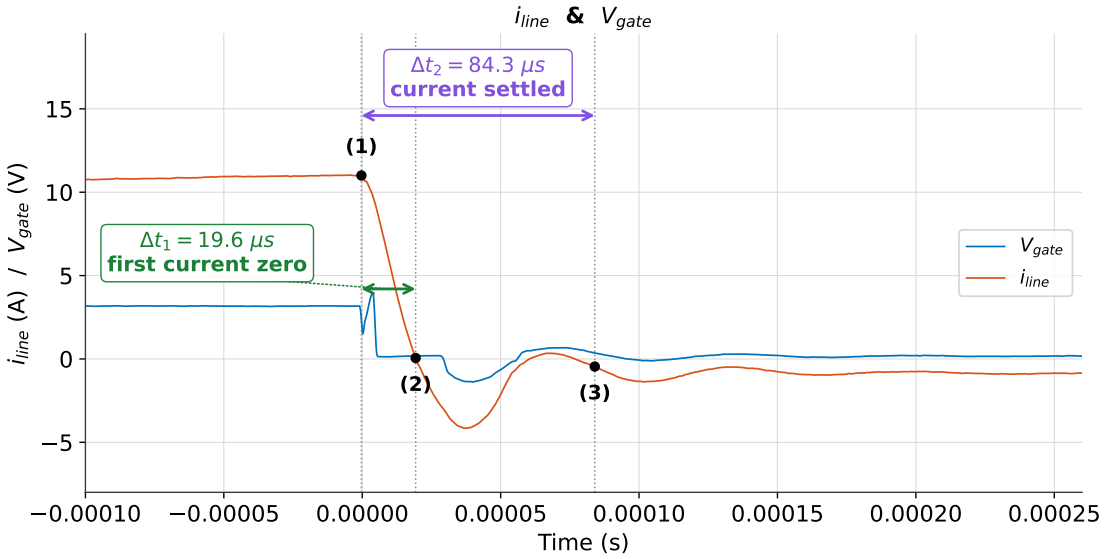
8.2 Πειράματα και αποτελέσματα

(α) Διακοπή με χειροκίνητο διακόπτη. Με το φορτίο ρυθμισμένο σε $10\,\mathrm{A_{rms}}$, ο διακόπτης διέκοψε το ρεύμα σχεδόν στην κορυφή αρνητικής ημιπεριόδου ($-14{,}20\,\mathrm{A}$), δηλαδή στην πλέον απαιτητική στιγμή. Ορίστηκαν δύο μεγέθη: ο χρόνος μέχρι τον πρώτο μηδενισμό $\Delta t_1 = 30{,}5\,\mu\mathrm{s}$, ο οποίος καθορίζει τη μέγιστη καταπόνηση και την ενέργεια που πρέπει να απορροφήσει ο κλάδος ψαλιδισμού, και ο χρόνος αποκατάστασης $\Delta t_2 = 83{,}1\,\mu\mathrm{s}$, ορισμένος ως η τελευταία στιγμή κατά την οποία το ρεύμα απέχει από την τελική του τιμή περισσότερο από $5\,\%$ του διακοπτόμενου ρεύματος. Η διάκριση έχει πρακτική σημασία: η αναφορά μόνο του Δt_1 θα υποτιμούσε τον χρόνο διακοπής κατά σχεδόν τρεις φορές. Κατά το μεταβατικό η τάση απαγωγού–πηγής έφτασε τα $-218\,\mathrm{V}$, πολλαπλάσιο της τάσης τροφοδοσίας — ακριβώς το φαινόμενο που καθιστά τον κλάδο απορρόφησης ενέργειας απαραίτητο.

(β) Αυτόματη αποκοπή με μικροεπεξεργαστή Texas Instruments. Με φορτίο $5\,\mathrm{A_{rms}}$ και κατώφλι λογισμικού $11\,\mathrm{A}$, μετρήθηκαν $\Delta t_1 = 19{,}6\,\mu\mathrm{s}$ και $\Delta t_2 = 84{,}3\,\mu\mathrm{s}$. Ο πρώτος μηδενισμός επιτυγχάνεται ταχύτερα, όπως αναμένεται από το μικρότερο διακοπτόμενο ρεύμα, ενώ οι χρόνοι αποκατάστασης είναι πρακτικά ταυτόσημοι με το χειροκίνητο πείραμα. Αυτό είναι το φυσικά αναμενόμενο: η ταλάντωση μετά τον μηδενισμό καθορίζεται από τη χωρητικότητα εξόδου, το κύκλωμα απόσβεσης και την παρασιτική επαγωγή του βρόχου,

μεγέθη που δεν αλλάζουν μεταξύ των δύο δοκιμών. Η αντικατάσταση του χειριστή από ελεγκτή με επεξεργαστή δεν υποβαθμίζει καθόλου τη διακοπή.

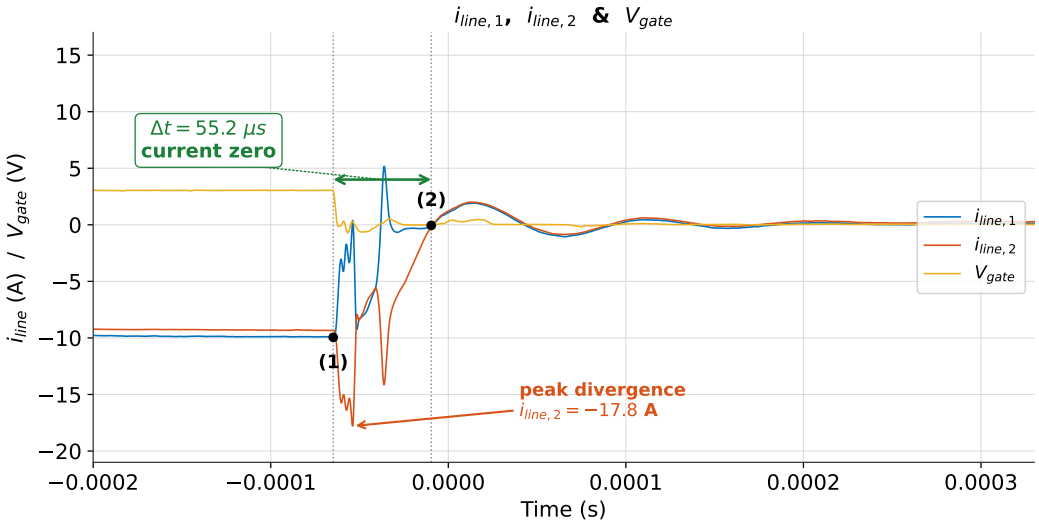
Στο Σχήμα Π.5 η απόκριση μετράται από την απόσυρση της εντολής πύλης· δεν περιλαμβάνεται η προηγούμενη καθυστέρηση ανίχνευσης.



Σχήμα Π.5. Πειραματική αυτόματη αποκοπή με κατώφλι στιγμιαίου ρεύματος 11 A*: πρώτος μηδενισμός στα* 19,6 μs *και αποκατάσταση στα* 84,3 μs *μετά την εντολή.*

(γ) Παράλληλη λειτουργία δύο μονάδων. Δύο πλακέτες συνδέθηκαν παράλληλα με κοινή εντολή πύλης, με φορτίο 12 A_{rms} και κατώφλι 10 A στη μία μόνο μονάδα. Κατά την αγωγή ο διαμοιρασμός του ρεύματος είναι: 5,93 έναντι 5,64 A_{rms}, δηλαδή ανισοκατανομή περίπου 5 %, χωρίς καμία ενεργό εξισορρόπηση. Κατά το μεταβατικό σβέσης, όμως, η συμφωνία καταρρέει: ενώ ο ένας κλάδος κινείται προς +5,2 A, ο δεύτερος οδηγείται στα −17,8 A, σχεδόν διπλάσιο του ρεύματος που έφερε πριν τη διακοπή. Παρατηρήθηκε ευαισθησία στη φυσική διασύνδεση, καθώς αλλαγή του μήκους ενός καλωδίου άλλαζε αισθητά το μοτίβο. Η παρατήρηση αυτή δεν απομονώνει, όμως, τον κυρίαρχο μηχανισμό. Πιθανές συνεισφορές είναι οι παρασιτικές εμπεδήσεις, τα ρεύματα των κυκλωμάτων απόσβεσης και περιορισμού τάσης, καθώς και διαφορές στην τοπική οδήγηση των πυλών. Η κοινή εντολή του ελεγκτή δεν αποδεικνύει ίδιες κυματομορφές πύλης–πηγής στις δύο πλακέτες. Επίσης, τα μετρούμενα εξωτερικά ρεύματα των κλάδων δεν διαχωρίζουν το ρεύμα των κύριων ημιαγωγών από εκείνο των παράλληλων κυκλωμάτων. Απαιτούνται στοχευμένες μετρήσεις για την επιβεβαίωση των αιτιών. Το τεκμηριωμένο συμπέρασμα είναι ότι ο καλός διαμοιρασμός στην αγωγή δεν εγγυάται ίδια μεταβατική απόκριση: χρειάζεται προσοχή στη συμμετρία των διαδρομών ισχύος και ελέγχου και έλεγχος της καταπόνησης κάθε μονάδας κατά τη διακοπή.

Στο Σχήμα Π.6 φαίνονται τα μετρούμενα ρεύματα των δύο παράλληλων κλάδων κατά την αποκοπή. Η κοινή εντολή πύλης συνοδεύεται από διαφορετικές μεταβατικές κυματομορφές, με κορυφή −17,8 A στον δεύτερο κλάδο πριν από τον πρώτο κοινό μηδενισμό.



Σχήμα Π.6. Εργαστηριακή παράλληλη λειτουργία δύο μονάδων: ρεύματα κλάδων και κοινή εντολή πύλης κατά την αποκοπή. Ο πρώτος κοινός μηδενισμός εμφανίζεται 55,2 μs μετά την απόσυρση της εντολής, με άνιση μεταβατική απόκριση των κλάδων.

(δ) Μέτρηση χρόνου απόκρισης. Απομονώθηκε η καθυστέρηση που εισάγει η ψηφιακή αλυσίδα ελέγχου. Το πραγματικό ρεύμα καταγράφηκε ταυτόχρονα από δύο ανεξάρτητα κανάλια: ένα κανάλι αναφοράς με αμπεροτσιμπίδα και ένα κανάλι δοκιμής, που προκύπτει από δειγματοληψία, επεξεργασία στο PLECS με βήμα T_s και ανακατασκευή μέσω του μετατροπέα ψηφιακού–αναλογικού. Η καθυστέρηση εξήχθη από τη διαφορά φάσης στη θεμελιώδη συχνότητα, $\hat{\tau} = -\Delta\varphi(f_0)/(2\pi f_0)$, μέθοδος της οποίας η ικανότητα διάκρισης δεν περιορίζεται από την περίοδο δειγματοληψίας του παλμογράφου. Δύο συνεισφορές κλιμακώνονται με το βήμα: $T_s/2$ από τη συγκράτηση μηδενικής τάξης και $1 \cdot T_s$ από τη διοχέτευση ενός βήματος του παραγόμενου κώδικα, δηλαδή

$$\text{delay}(T_s) = \tfrac{1}{2}T_s + 1 \cdot T_s + t_0 = 1{,}5\,T_s + t_0.$$

Η προσαρμογή ελαχίστων τετραγώνων σε πέντε μετρήσεις, οι οποίες καλύπτουν εύρος $25\times$, έδωσε $1{,}50\,T_s + 18\,\mu$s· ο μετρούμενος συντελεστής αναπαράγει τον προβλεπόμενο 1,5 με σφάλμα κλάσματος της εκατοστιαίας μονάδας. Για σχεδιαστική χρήση προτείνεται το αυστηρό άνω φράγμα $\text{delay}(T_s) \le 1{,}5\,T_s + 50\,\mu$s, το οποίο ικανοποιείται από όλες τις μετρήσεις και επιτρέπει τον υπολογισμό της χειρότερης περίπτωσης χωρίς εξάρτηση από τις ακριβείς τιμές μιας παλινδρόμησης.

(ε) Σύγκριση με ηλεκτρομηχανικό επαφέα. Το ίδιο ρεύμα ($6\,\text{A}_{\text{rms}}$ στα $65\,\text{V}_{\text{rms}}$) διακόπηκε χρησιμοποιώντας έναν κύριο πόλο του τριπολικού επαφέα Schneider Electric TeSys D LC1D09P5 [5]. Η ουσιώδης διαφορά φαίνεται αμέσως: η τάση στις επαφές *δεν* ανεβαίνει για να απομονώσει την τροφοδοσία, αλλά παραμένει περίπου στο 1 V, επειδή μόλις χωρίζονται οι επαφές εμφανίζεται τόξο που κρατά το κύκλωμα κλειστό. Στα $t = 7{,}51$ ms το ρεύμα φτάνει στον φυσικό του μηδενισμό, όπου θα ανέμενε κανείς τη διακοπή — αλλά το διάκενο δεν έχει ακόμη ανακτήσει επαρκή διηλεκτρική αντοχή, το τόξο υπάρχει ακόμα και το ρεύμα συνεχίζει στην αντίθετη κατεύθυνση. Αυτό που τελικά

το σταματά δεν είναι μηδενισμός αλλά η αύξηση της ίδιας της τάσης του τόξου, η οποία μετρήθηκε στα $\approx 39\,\mathrm{V}$ στα $10{,}0\,\mathrm{ms}$ και $\approx 67\,\mathrm{V}$ στα $10{,}7\,\mathrm{ms}$, μειώνοντας προοδευτικά το ρεύμα. Το τόξο γίνεται μη διατηρήσιμο στα $t = 10{,}92\,\mathrm{ms}$.

Ο λόγος των χρόνων μέχρι τον τελικό μηδενισμό είναι $10{,}91\,\mathrm{ms}$ έναντι $0{,}139\,\mathrm{ms}$, δηλαδή $78\times$. Ο λόγος της *διερχόμενης ενέργειας* $\int i^2\,\mathrm{d}t$, όμως, είναι $0{,}348\,\mathrm{A^2s}$ έναντι $3{,}39 \times 10^{-4}\,\mathrm{A^2s}$, δηλαδή περίπου $1000\times$. Η δυσαναλογία εξηγείται από το ότι η διερχόμενη ενέργεια εξαρτάται από το *τετράγωνο* του ρεύματος και ότι οι δύο διατάξεις δεν διακόπτουν στο ίδιο σημείο της κυματομορφής. Ο Πίνακας Π.4 συνοψίζει τα πειραματικά αποτελέσματα.

Πίνακας Π.4. Σύνοψη των πειραματικών αποτελεσμάτων.

Πείραμα	**Συνθήκες**	**Βασικό αποτέλεσμα**
Χειροκίνητη διακοπή	$10\,\mathrm{A_{rms}}$, διακοπή στην κορυφή	$\Delta t_1 = 30{,}5\,\mu\mathrm{s}$, $\Delta t_2 = 83{,}1\,\mu\mathrm{s}$
Αυτόματη αποκοπή με μικροεπεξεργαστή	$5\,\mathrm{A_{rms}}$, κατώφλι $11\,\mathrm{A}$	$\Delta t_1 = 19{,}6\,\mu\mathrm{s}$, $\Delta t_2 = 84{,}3\,\mu\mathrm{s}$
Παράλληλη λειτουργία	$12\,\mathrm{A_{rms}}$, κοινή εντολή	Ανισοκατανομή $\approx 5\,\%$ στην αγωγή· $-17{,}8\,\mathrm{A}$ στο μεταβατικό
Χρόνος απόκρισης	$T_s = 20$–$500\,\mu\mathrm{s}$	delay $\approx 1{,}50\,T_s + 18\,\mu\mathrm{s}$
Σύγκριση με επαφέα	$6\,\mathrm{A_{rms}}$	$78\times$ ταχύτερη διακοπή· $\approx 1000\times$ μικρότερη $\int i^2\mathrm{d}t$

9. Προκλήσεις, ανοιχτά ζητήματα και μελλοντικές κατευθύνσεις

Παρά την αξιοσημείωτη πρόοδο της τελευταίας δεκαετίας, αρκετά ανοιχτά ζητήματα εμποδίζουν σήμερα την επικράτηση των διακοπτών στερεάς κατάστασης στην πλειονότητα των εφαρμογών διανομής.

Οι απώλειες αγωγής και η διαχείριση θερμότητας παραμένουν ο σημαντικότερος περιορισμός: ακόμη και με τα πιο προηγμένα SiC MOSFET, η πτώση τάσης στο ονομαστικό ρεύμα είναι 1–2 V, δηλαδή ένα έως δύο watt ανά αμπέρ. Για διακόπτη 600 A, στον οποίο ένας πόλος απαιτεί δύο στοιχεία στη διαδρομή του ρεύματος, αυτό σημαίνει έκλυση 1–2 kW ανά πόλο και συνεπώς υπερδιαστασιολογημένη ψύκτρα ή ενεργή ψύξη. Η αντοχή του κλάδου απορρόφησης ενέργειας είναι περιορισμός ειδικός για την τεχνολογία: ο ημιαγωγός αντέχει εκατομμύρια χειρισμούς, το βαρίστορ όμως όχι. Ακολουθούν το κόστος και η τυποποίηση — με την εκπόνηση διεθνών προτύπων από ομάδες εργασίας της IEC και του IEEE σε εξέλιξη. Η κλιμάκωση με σειριακή και παράλληλη σύνδεση, που εγείρει ζητήματα κατανομής τάσης και ρεύματος αντίστοιχα — όπως επιβεβαίωσε πειραματικά η παρούσα εργασία. Η ενσωμάτωση με ψηφιακή προστασία και επικοινωνίες. Ο συντονισμός με την υπάρχουσα προστασία και η αυτόματη επαναφορά, όπου η ίδια η ταχύτητα του διακόπτη δημιουργεί νέα ζητήματα, όπως η αποφυγή ανεπιθύμητης λειτουργίας κατά τα ρεύματα εκκίνησης. Τέλος, η εξέλιξη προς ευφυείς και αυτοτροφοδοτούμενους διακόπτες. Ο συντονισμός πρέπει επίσης να λαμβάνει υπόψη τις εφαρμοστέες απαιτήσεις

αδιάλειπτης λειτουργίας σε βύθιση τάσης (LVRT) των μονάδων παραγωγής [3]. Εφόσον χρησιμοποιείται περιορισμός ρεύματος κατά το απαιτούμενο χρονικό διάστημα, το MOV πρέπει να αντέχει τη σωρευτική ενέργεια των επαναλαμβανόμενων παλμών, με συνεκτίμηση της ψύξης του. Η παρούσα μελέτη δεν τεκμηριώνει συμμόρφωση με απαιτήσεις LVRT.

Ως κατευθύνσεις συνέχειας προτείνονται: πλήρες, βαθμονομημένο ηλεκτροθερμικό μοντέλο που να λαμβάνει υπόψη και τα δύο στοιχεία του αντι-σειριακού ζεύγους, ποσοτικός υπολογισμός της ενέργειας κάθε πόλου στο τριφασικό μοντέλο, με σάρωση της χρονικής στιγμής σφάλματος και επαναληπτικές προσομοιώσεις ανοχών με δηλωμένες τυπικές αποκλίσεις, ώστε η άνιση καταπόνηση των βαριστόρ να τεκμηριωθεί αριθμητικά, διερεύνηση τοπολογίας μέσης τάσης με σειριακή σύνδεση στοιχείων και ενεργή εξισορρόπηση τάσης και πειραματική υλοποίηση του ενεργού περιορισμού ρεύματος με τη διαδρομή ελεύθερης εκφόρτισης, η οποία εδώ μελετήθηκε μόνο σε προσομοίωση.

10. Συμπεράσματα

Η εργασία κάλυψε τον πλήρη κύκλο μελέτης ενός διακόπτη ισχύος στερεάς κατάστασης για εφαρμογές εναλλασσόμενου ρεύματος: από τη βιβλιογραφική ανασκόπηση των τεχνολογιών διακοπής και των ημιαγωγικών στοιχείων, στη μοντελοποίηση και προσομοίωση μονοφασικών και τριφασικών συστημάτων, και τελικά στην πειραματική επαλήθευση σε εμπορική πλακέτα αξιολόγησης. Τα κύρια συμπεράσματα συνοψίζονται ως εξής. Πρώτον, το πλεονέκτημα ταχύτητας του διακόπτη στερεάς κατάστασης δεν είναι ποσοτικό αλλά ποιοτικό: στην προσομοίωση, το μέγιστο διερχόμενο ρεύμα μειώθηκε από 1260 A σε 100 A και ο χρόνος διακοπής από 36 ms σε 0,8 ms έναντι του ηλεκτρομηχανικού διακόπτη, ενώ πειραματικά η διερχόμενη ενέργεια μειώθηκε κατά τρεις τάξεις μεγέθους. Δεύτερον, ο ενεργός περιορισμός ρεύματος είναι εφικτός για τον ημιαγωγό, αλλά είναι *ασύμβατος* με ένα συμβατικό βαρίστορ μονού παλμού: χωρίς πρόβλεψη διαδρομής εκφόρτισης, η σωρευτική ενέργεια του βαριστόρ ξεπερνά κατά τριάντα φορές εκείνη μιας άμεσης διακοπής. Η ελεγχόμενη διαδρομή ελεύθερης εκφόρτισης που προτάθηκε επαναφέρει την ενέργεια αυτή σε επίπεδα μίας μόνο διακοπής. Τρίτον, σε τριφασικό περιβάλλον η κοινή εντολή σβέσης δεν συνεπάγεται κοινή καταπόνηση: κάθε φάση πρέπει να διαστασιολογείται για τη χειρότερη μονοφασική ενέργεια. Τέταρτον, η ταχεία διακοπή της συνεισφοράς μιας τοπικής σύγχρονης γεννήτριας απαλείφει την ταλάντωση ροπής και την υπερδιέγερση που εμφανίζονται με βραδύτερο διακόπτη. Η πιθανή αξιοποίηση για αύξηση της ικανότητας φιλοξενίας παραγωγής απαιτεί ξεχωριστή μελέτη προστασίας και συμβατότητας με τις απαιτήσεις LVRT. Πέμπτον, στο πειραματικό επίπεδο, ο έλεγχος μέσω επεξεργαστή δεν υποβαθμίζει καθόλου τη δυναμική της διακοπής, η καθυστέρηση της ψηφιακής αλυσίδας περιγράφεται πλήρως από τον νόμο $1{,}5\,T_s$, ενώ στην παράλληλη σύνδεση παρατηρήθηκαν άνισα εξωτερικά ρεύματα κλάδων κατά τη σβέση, παρά την κοινή εντολή οδήγησης. Η αιτία δεν απομονώθηκε και απαιτείται έλεγχος της μεταβατικής καταπόνησης κάθε μονάδας, με συνεξέταση της διασύνδεσης, της οδήγησης και των κυκλωμάτων απόσβεσης. Το κύριο εμπόδιο παραμένει οικονομικό και θερμικό, όχι λειτουργικό: οι απώλειες αγωγής και το κόστος των ημιαγωγών ευρέος διακένου. Καθώς και τα δύο βελτιώνονται σταθερά, ο διακόπτης στερεάς κατάστασης αναμένεται να εξελιχθεί από παθητική διάταξη προστασίας σε ενεργό κόμβο του ευφυούς δικτύου.

Chapter 1

Introduction

1.1 Motivation and background

The protection of electric power systems has historically relied on electromechanical circuit breakers, which combine simple operating principles with very low conduction losses and excellent reliability. For more than a century these devices have been the only practical means of interrupting fault currents in AC networks at virtually every voltage class. Yet the electric power system itself is changing. Industrial and residential loads are being increasingly electrified, the proportion of power-electronic equipment inside the grid is growing at an accelerating pace, electric vehicles and fast-charging infrastructure are entering the distribution network in large numbers, and distributed generation from renewable energy sources has shifted the once-passive distribution feeder into an active, bidirectional system. In parallel, end-users expect an ever higher quality of supply and a lower tolerance for outages, particularly in data centers, industrial automation and critical infrastructure [2, 6].

These trends place new and more demanding requirements on the protection chain. Power-electronic converters, which today represent a significant share of the connected load and an even larger share of the new generation capacity, exhibit very limited short-circuit withstand capability and require protection times on the order of a few milliseconds or less. The widespread adoption of distributed generation also changes the magnitude, direction and waveform of the fault currents that the breakers have to interrupt, complicating the coordination of conventional time-overcurrent protection schemes [2, 7]. At the same time, the move toward digital, communications-based substations imposes additional requirements on the controllability and observability of the protection equipment [8].

Conventional electromechanical breakers, despite their maturity, cannot meet all these requirements simultaneously. Their clearing time, typically in the range of 30–80 ms, is incompatible with the protection of sensitive power-electronic equipment; their mechanical contacts wear out and require periodic maintenance; the arc they produce limits their use in confined or hazardous environments. These limitations have motivated significant research interest in faster, more flexible and more intelligent protection devices, of which the *solid-state circuit breaker* (SSCB) is currently one of the most actively researched candidates for low- and medium-voltage applications [2].

1.2 The role of the circuit breaker in modern grids

A circuit breaker is the element of the protection chain that is ultimately responsible for interrupting fault currents and isolating the faulted section of the network. Electromechanical breakers achieve this by mechanically separating a pair of metallic contacts

and extinguishing the resulting electric arc using oil, SF_6, vacuum or air as an insulating medium. Electromechanical breakers have several properties that are hard to match: very low conduction losses during normal operation (the contact resistance is typically below 100 $\mu\Omega$ for molded-case and air circuit breakers, and a few milliohms for miniature circuit breakers), virtually unlimited voltage scalability, and a long service lifetime when used at moderate switching rates. However, they also have well-known limitations: the operating times mentioned above, the mechanical wear of the contacts, the need for periodic maintenance, the large physical volume, and the production of an arc that limits their use in some environments [2, 9].

Solid-state circuit breakers, on the other hand, replace the mechanical contacts with one or more controllable semiconductor switches such as IGBTs, IGCTs, SiC MOSFETs or SiC JFETs [10]. They can interrupt the current within microseconds, are inherently free of moving parts, do not produce an arc, and can be operated millions of times without significant aging of the switching elements [2]. These advantages are particularly valuable in applications where the protected system contains power-electronic converters with limited short-circuit withstand capability, where mechanical breakers are too slow, or where mechanical complexity must be minimized. The continuous improvement of wide-bandgap (WBG) semiconductors, in particular silicon carbide (SiC), has substantially increased the voltage and current ratings achievable with practical solid-state designs, opening the door to commercial AC SSCB products for low-voltage distribution [11, 12] and to laboratory prototypes for medium-voltage applications [13].

The main drawback of solid-state breakers is the conduction loss associated with the on-state voltage drop of the semiconductor switches. Even with modern devices, the on-state voltage is on the order of 1–3 V, which translates into significant continuous losses for currents of hundreds or thousands of amperes. Mitigating this loss is one of the main areas of active research, together with cost reduction, miniaturization, thermal management and standardization [2, 14].

1.3 Objectives of this thesis

Against this background, this thesis investigates the use of solid-state circuit breakers in AC power systems, with particular emphasis on low-voltage distribution applications. The main objectives of the work are:

- To present a structured overview of modern AC power systems and the protection challenges that arise from their continuing evolution, with attention to the role played by electrification, power-electronic loads and distributed generation.
- To review and compare the main circuit-breaker technologies currently used or proposed in the literature—electromechanical, hybrid, resonant and solid-state—and to clarify the regions of operation for which each technology is best suited.
- To examine in detail the families of power semiconductor devices that can be used in the realization of solid-state circuit breakers, with particular attention to their operating principles, their static and dynamic characteristics, and their respective advantages and limitations.

- To analyze the architecture and operating principle of solid-state circuit breakers and to discuss the principal AC SSCB topologies proposed in the literature, together with their auxiliary subsystems.
- To investigate, through simulation in MATLAB/Simulink, the behavior of representative SSCB topologies in single-phase and three-phase AC systems under normal operating conditions and during typical fault scenarios.
- To validate the SSCB concept experimentally on a commercially available evaluation platform, and to characterize aspects of its practical operation – such as processor-based control, parallel operation of multiple units and overall response time – that complement the theoretical and simulation-based analysis.

The thesis therefore spans the full arc of the subject: a critical comparison of the competing protection technologies, a modeling and simulation study of the resulting design trade-offs, and an experimental validation of the concept on commercial hardware.

1.4 Thesis outline

The remainder of this document is organized as follows. Chapter 2 introduces modern AC power systems and discusses the operational and protection challenges that arise from their ongoing evolution, including a dedicated section on the integration of renewable energy sources. Chapter 3 examines the fault behavior of AC systems and the contributions of the different fault-current sources that may be encountered in a contemporary distribution feeder. Chapter 4 reviews the main families of circuit-breaker technologies (electromechanical, hybrid, resonant and solid-state) and provides a comparative summary. Chapter 5 is devoted to the power semiconductor devices that can be used in SSCB realizations; each device family is analyzed in detail and a comparative discussion is provided. Chapter 6 focuses on the SSCB itself: generic architecture, operating principle, AC topologies, auxiliary circuits and representative applications. Chapter 7 presents the modeling and simulation work: a single-phase test circuit used to study direct interruption, current limiting and the energy absorbed by the clamping varistor, followed by a three-phase distribution network studied with passive loads and with a local synchronous generator. Chapter 8 presents the experimental validation of the SSCB concept on a commercial evaluation platform, describing the test setup and the experiments that were carried out. Chapter 9 summarizes the main open challenges and the future directions for SSCB technology.

Chapter 2

Modern AC Power Systems and Protection Challenges

AC three-phase power systems have been the dominant form of electric power transmission and distribution worldwide for more than a century. Their success rests on two technological cornerstones: the transformer, which allows efficient stepping-up and stepping-down of voltage levels, and the synchronous machine, which provides a robust voltage source with substantial rotational inertia. For decades the structure of these systems was largely uniform: large, centralized power plants located near primary energy resources fed power through long high-voltage transmission lines to step-down substations and from there, through radial distribution feeders, to predominantly passive loads. Protection coordination, voltage regulation and frequency control were designed under this paradigm.

Over the last two decades several simultaneous developments have started to challenge this picture. Industrial automation, building electrification, information technology infrastructure and the rise of electric mobility have profoundly changed the nature and the dynamics of the loads connected to the grid. At the same time, the shift from rotating machines to power-electronic converters as the dominant interface between primary energy sources and the grid, along with the rapid growth of distributed generation, has transformed the distribution network from a passive recipient of energy into an active, bidirectional system. The implications for the design and operation of power systems—and especially for their protection—are far-reaching and have motivated significant research and engineering effort. This chapter reviews those of these developments that are most relevant to the design of modern protection devices, and in particular of solid-state circuit breakers.

2.1 The evolution of AC distribution networks

The structure of low- and medium-voltage AC distribution networks was, until recently, very stable. Industrial plants drew power from medium-voltage feeders through dedicated step-down transformers, residential and commercial buildings were fed by radial low-voltage feeders, and the loads themselves were dominated by linear loads (incandescent lighting, resistive heating and directly connected induction motors), with only a small share of power-electronic appliances. Protection of these networks relied mainly on time-overcurrent relays and fuses at the medium-voltage level, and on thermal-magnetic miniature circuit breakers (MCBs) and fuses at the low-voltage level, with arc-extinction times of several tens of milliseconds being entirely acceptable for the dominant electromechanical and thermal loads.

In modern AC distribution networks, the same backbone is being asked to feed a

much wider variety of loads and to host an increasing number of sources. The ratio between peak and average load has grown as a result of the electrification of heating, cooling and cooking, and the addition of electric vehicle (EV) charging at residential level. Industrial facilities increasingly rely on variable-speed drives, controllable rectifiers and uninterruptible power supplies, all of which behave as nonlinear, controllable loads with strict requirements on power quality. Critical infrastructure such as data centers, hospitals, semiconductor fabs and railway substations demands uninterrupted, high-quality supply with stringent voltage and frequency tolerances. Together, these trends have raised the bar that any protection device must meet, in terms of speed, selectivity, controllability and reliability [2, 6].

Figure 2.1 contrasts the two situations. In the traditional feeder of Figure 2.1(a) there is a single source of fault current and it always flows in the same direction, which is what makes a graded set of overcurrent thresholds a sufficient protection scheme. In the feeder of Figure 2.1(b) neither assumption survives: several sources can feed the same fault from either direction, and the converter-interfaced ones contribute a current only marginally above their rated value.

2.2 The shift to power-electronic interfaces

Perhaps the most important single change in modern AC systems is the proliferation of static power-electronic converters as the primary interface between sources, loads and the grid. The reasons for this proliferation are many: photovoltaic plants, full-converter wind turbines and battery energy storage systems all produce DC power that must be inverted to AC; EV chargers, data-center power supplies and industrial drives benefit from the efficiency and controllability of converter-based interfaces; and high-voltage direct current (HVDC) links connect entire regions of the AC grid through power-electronic terminals.

Compared with the rotating machines that they progressively displace, voltage-source converters (VSCs) exhibit several distinctive features that are highly relevant for protection design [2, 7]. Firstly, they have very small electrical inertia: their output current can change much faster than the rotor of a synchronous machine, but the maximum current they can deliver is strictly limited by the rated current of their semiconductor switches. Secondly, their behavior during faults is determined primarily by their control algorithm rather than by circuit impedances alone: typical implementations limit the short-circuit current contribution to 1.1–1.5 p.u. of the rated current and to sustain this limited current for the duration required by the fault ride-through requirements of the grid code, blocking only if the fault persists beyond it. Thirdly, converters are inherently controllable: their switching elements can be turned on and off within microseconds, which allows a wide range of advanced functions (active and reactive power control, fault ride-through, harmonic compensation, virtual inertia emulation), but also means that the system is more vulnerable to the loss of the converters if they shut down to protect themselves. These controlled current limits do not bound every initial transient: short-duration peaks depend on the converter topology, filters and protection

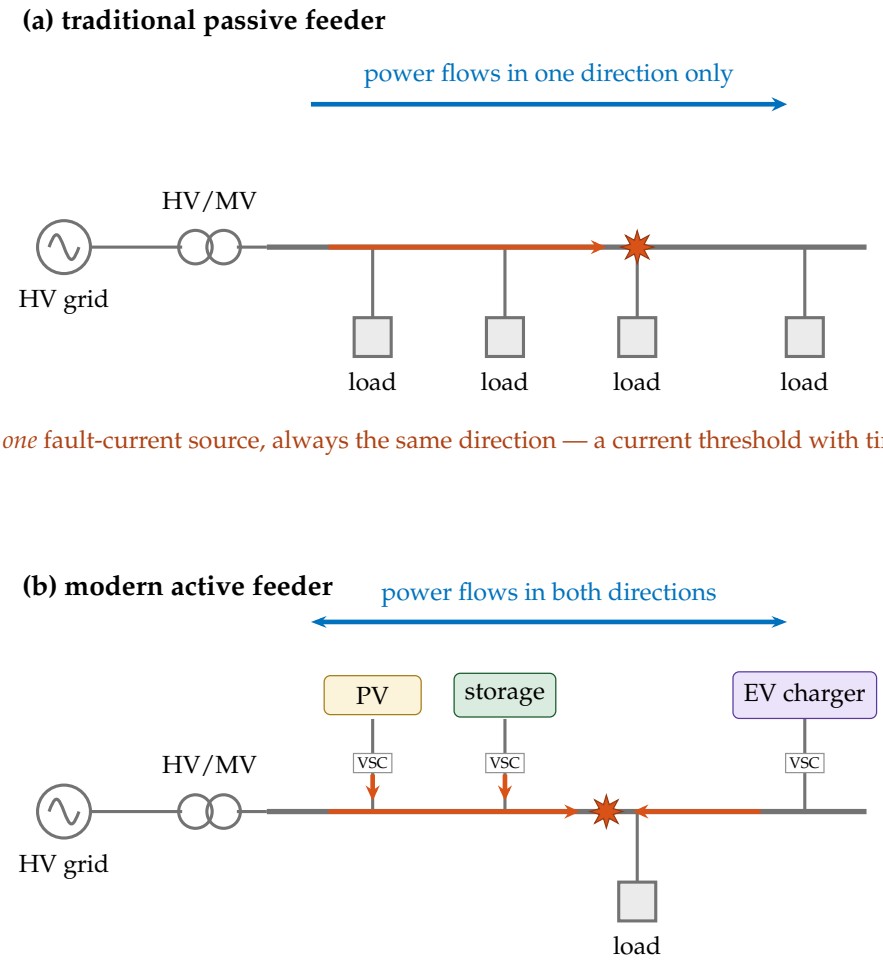


Figure 2.1. Evolution of the low- and medium-voltage distribution feeder. (a) The traditional passive feeder: one source, radial flow, and a fault current that is both large and unidirectional. (b) The contemporary active feeder, hosting distributed generation, storage and electric-vehicle charging behind voltage-source converters: power flows in both directions and a fault is fed from several points at once, each converter contributing only 1.1–1.5 *p.u.*

response [15]. Under unbalanced faults, the controller can also shape the sequence composition of the current: some strategies suppress the negative-sequence component, whereas others deliberately inject a controlled negative-sequence current. Sequence suppression is therefore control-dependent, not a universal inverter characteristic [1].

These properties shape the requirements of the protection chain in two fundamental ways. First, the protection device must be able to detect and clear faults much faster than the short-circuit withstand time of the converters, which is typically in the millisecond range; conventional electromechanical breakers, with clearing times of tens of milliseconds, are simply too slow. Second, the protection device must be able to discriminate between true faults and the much smaller fault-current contributions of inverter-based sources, which may be only marginally distinguishable from normal load currents [8, 15].

2.3 Renewable energy integration

Distributed generation from renewable energy sources is one of the most visible and most rapidly growing manifestations of the power-electronic revolution discussed above. According to the International Renewable Energy Agency [16], the installed capacity of renewable energy worldwide more than doubled in the decade between 2015 and 2025, growing from 1,985 GW to 5,149 GW, with photovoltaic (PV) systems and wind farms accounting for the bulk of the new additions. Residential and commercial rooftop PV installations alone now exceed several hundred gigawatts of installed capacity, and the trend is strongly upward.

The integration of renewable distributed generation into existing distribution networks brings well-documented benefits: it reduces transmission losses, defers investments in new transmission and distribution infrastructure, increases resilience by allowing islanded operation of portions of the network, and contributes to the decarbonization of electricity supply. On the technical side, however, the connection of significant amounts of distributed generation to networks that were not originally designed for it raises a number of issues including [8, 15]:

- Bidirectional power flow on feeders that were traditionally designed as radial and unidirectional, requiring revision of voltage-regulation strategies and protection settings.
- Local voltage rise during periods of high generation and low local consumption, particularly at the end of long rural feeders.
- Increased harmonic distortion caused by switching converters, especially when many small units are aggregated on the same feeder.
- Altered fault levels – increased at the point of connection, but with a reduced and direction-dependent contribution seen by upstream relays – which cause protection blinding and sympathetic tripping and complicate overcurrent coordination.
- Anti-islanding requirements that introduce additional constraints on the converter control algorithms and on the protection scheme.

From the standpoint of protection design, the most important of these issues are the change in fault-current magnitude and direction, and the consequent need for much faster and more selective protection. Fast, fully controllable SSCBs are an enabling technology in this context: they allow individual converters and strings to be protected without affecting the rest of the plant, enable seamless transition between grid-connected and islanded operation, and support the implementation of adaptive protection schemes that follow the changing topology of the active distribution network [17]. Renewable integration is therefore one of the strongest drivers, but by no means the only one, of the current research interest in solid-state circuit breakers.

2.4 Microgrids and active distribution networks

A microgrid is a local electric power system that combines distributed generation, energy storage and controllable loads, and that is capable of operating either connected to the main grid (grid-connected mode) or in isolation from it (islanded mode). The microgrid concept emerged in the early 2000s as a way of organizing the integration of distributed energy resources at the distribution level, and has since been adopted in a variety of contexts ranging from university campuses and military bases to entire industrial complexes and remote communities [8, 18].

From an architectural perspective, microgrids can be classified as AC, DC, or hybrid AC/DC, depending on the type of bus used to interconnect the various resources. AC microgrids retain compatibility with existing AC infrastructure and standards but require synchronization of all converters and benefit less from the natural DC character of PV panels and batteries. DC microgrids eliminate synchronization and reactive-power management issues and can be more efficient when most sources and loads are DC in nature, but require the development of new DC protection devices and standards [19, 20]. Hybrid AC/DC microgrids combine the two structures and are often considered the most flexible solution for future systems [8].

Regardless of the bus topology, the operation of microgrids—and more generally of active distribution networks containing significant amounts of distributed generation and storage—imposes much more stringent requirements on the protection devices than those typical of conventional passive distribution networks. Selectivity, sensitivity and speed must all be improved simultaneously, and protection must remain effective under operating conditions that may differ substantially from one moment to the next (e.g., grid-connected versus islanded mode, high versus low local generation, motor starting transients, EV-charging inrush). It is precisely in such contexts that solid-state circuit breakers are expected to find their natural domain of application, providing protection at the level of individual feeders, individual converters, or individual loads, and enabling fast, autonomous reconfiguration of the network in response to faults [19].

2.5 General protection challenges in modern AC systems

The trends discussed in the previous sections combine to define a set of interrelated protection challenges that conventional schemes are not always well equipped to address [2, 7, 8]:

- **Mismatch between protection speed and load sensitivity.** Power-electronic equipment—variable-speed drives, EV chargers, UPS units, telecom rectifiers, and inverter-based generation—has a very limited short-circuit withstand capability, typically in the millisecond range. Electromechanical breakers with 30–80 ms clearing time cannot prevent damage to such equipment during severe faults; fast tripping by SSCBs reduces the let-through energy and improves the survival rate of downstream components.
- **Bidirectional power flow.** Distributed generation, energy storage and vehicle-to-

grid systems can cause power to flow in either direction along a feeder. Directional protection elements must be added or reconfigured, and the coordination of breakers must be re-examined.

- **Variable and source-limited fault levels.** Both the magnitude and the angle of the fault current depend on the number of inverter-based resources currently connected and on their control mode. Protection settings that are optimal under one operating condition may become inadequate when the topology or the generation mix changes [15].
- **Inrush and load-transient discrimination.** Modern AC systems feature increasingly frequent and severe transient phenomena—motor starting, transformer energization, capacitor-bank switching, EV-charger inrush—whose initial current peaks may be comparable to moderate fault currents. The protection device must combine sensitivity with discrimination, ideally exploiting waveform features such as the current rate of rise rather than the magnitude alone.
- **Power-quality and continuity requirements.** Data centers, semiconductor manufacturing and other process industries require clearing times short enough to avoid the propagation of voltage sags to sensitive loads. Reclosing schemes must also be fast and reliable to minimize the interruption time perceived by the end-user.
- **Anti-islanding and fault ride-through.** Grid-connection codes increasingly require distributed generators both to disconnect rapidly during anti-islanding events and to ride through short-duration faults without disconnecting. These contradictory requirements must be coordinated with the protection of the surrounding feeder [8].
- **Integration with digital protection and communications.** Modern protection schemes rely on IEC 61850 and similar standards to exchange measurement data and trip commands between protection devices in real time. The breaker must be able to participate in this communication, accept remote commands and report its own status.

These challenges have led to the development of new protection schemes based on communication-assisted differential protection, adaptive overcurrent protection, distance protection and centralized protection systems. Independently of the protection logic, however, the actual interruption of the fault must still be performed by a circuit breaker, and the speed and controllability of that breaker ultimately determine what the protection scheme can or cannot achieve. This is the main reason why solid-state circuit breakers are increasingly regarded as a key enabling technology for the protection of modern AC distribution systems—both those dominated by renewable distributed generation and those whose evolution is driven by electrification, by power-electronic loads or by the demand for higher power quality [6].

Chapter 3

Fault Behavior and Protection Requirements in AC Systems

The design of any protection device—and of a solid-state circuit breaker in particular—must start from a clear understanding of the fault phenomena that the device is supposed to interrupt. This chapter reviews the nature of short-circuit currents in AC systems, the contributions of the principal fault-current sources found in modern distribution feeders, and the resulting requirements that a contemporary AC protection system must satisfy [8, 9, 15].

3.1 Short-circuit currents in AC systems

In an AC system fed by synchronous generators or by a stiff upstream grid, a short circuit produces a current waveform that contains both an alternating component and, in general, a transient direct component related to the instant of fault occurrence. Using a simplified RL model, the fault-loop current can be written as

$$i(t) = \frac{V_m}{Z}\left[\sin(\omega t + \alpha - \varphi) - \sin(\alpha - \varphi)\, e^{-t\,R/L}\right], \tag{3.1}$$

where V_m is the peak driving voltage of the fault loop, Z and φ are the magnitude and angle of the loop impedance, α is the voltage phase angle at the instant of fault occurrence, and R/L is the inverse of the loop time constant. The first term represents the steady-state symmetrical component, while the second represents the transient DC offset. The peak instantaneous current may therefore be substantially higher than the steady-state value, especially when the fault occurs near a voltage zero crossing, which for the predominantly inductive loop impedances typical of power circuits gives the largest DC offset, as illustrated in Figure 3.1 [9].

The most important feature of this waveform for protection purposes is that, once the DC offset has decayed, the current crosses zero every half cycle. For faults with a large offset and a long loop time constant the first zero crossings may be delayed by several cycles, a condition for which mechanical breakers must be explicitly rated. This property has been exploited for over a century by AC mechanical circuit breakers, which open their contacts and rely on the natural zero crossing to extinguish the resulting electric arc. The combination of well-defined zero crossings, large and predictable fault currents, and tolerance of synchronous generators to short-duration overcurrents has been the basis of conventional AC overcurrent protection.

Faults in AC systems are conventionally classified into three-phase symmetric faults, line-to-line faults, double line-to-ground faults and single line-to-ground faults. The last category, the most frequent in real distribution networks, involves the zero-sequence network and is typically detected by dedicated ground-fault protection schemes. From

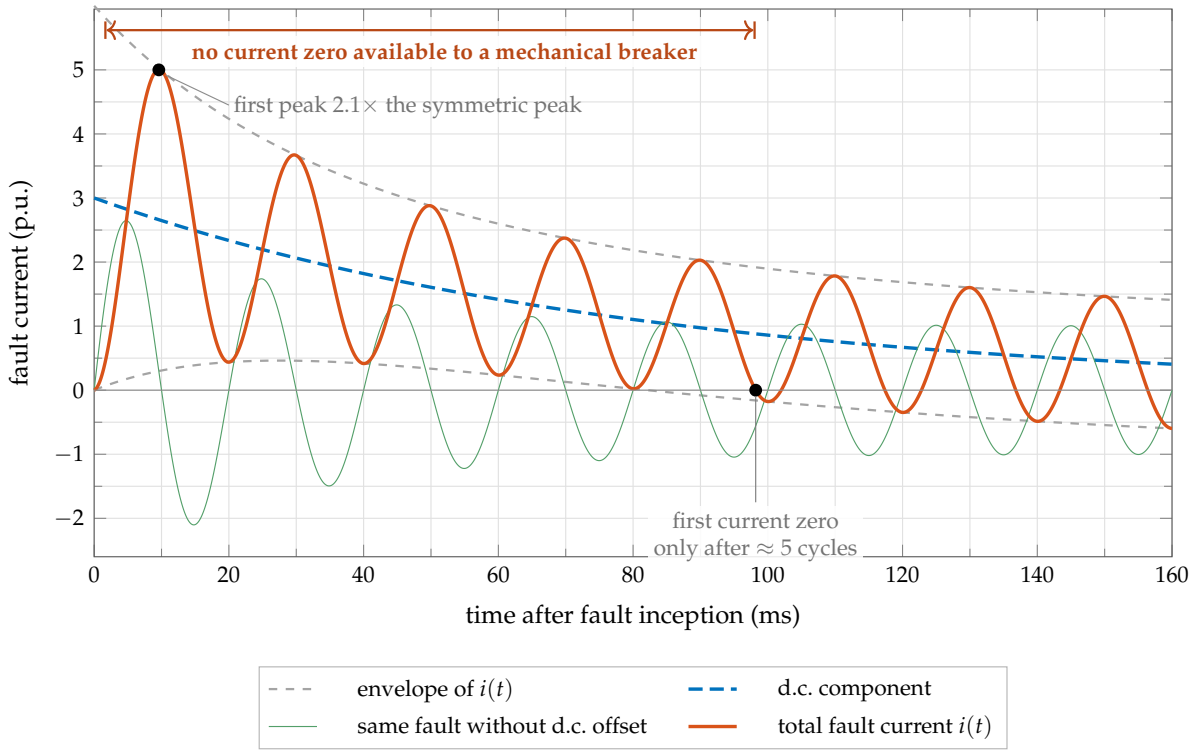


Figure 3.1. Asymmetrical short-circuit current for a fault initiated at the instant of maximum DC offset. The curve follows Equation (3.1)*, with the symmetrical component given a decaying amplitude so as to represent a machine-fed fault: it falls with the sub-transient and transient time constants of the machine, whereas the DC offset falls with the slower loop time constant L/R. Because the offset outlives the a.c. component, the total current keeps one polarity for about five cycles and offers no zero crossing at which a mechanical breaker could clear. The first peak reaches* 2.1 *times that of the same fault initiated without offset, shown for comparison.*

the standpoint of the breaker, all four fault types impose qualitatively similar requirements: the device must be able to interrupt currents that may be several times the rated current, with controlled overvoltage at the moment of interruption and with sufficient dielectric recovery to avoid re-strikes [9].

3.2 Fault-current sources in a contemporary distribution feeder

A contemporary low- or medium-voltage AC feeder may contain several different fault-current sources, each with its own dynamic characteristics; they are the sources shown schematically in Figure 2.1(b). The protection device must be designed to handle the worst-case combination of all of them. The most important sources, in approximate order of fault-current contribution, are:

The upstream grid. In a grid-connected feeder, the bulk of the fault current is supplied by the upstream transmission and sub-transmission network, which behaves approximately as a Thévenin-equivalent voltage source with a low impedance. The available

short-circuit current is dictated by the network impedance up to the point of common coupling and may reach tens of kiloamperes in a typical low-voltage installation. This current is sustained and contains well-defined zero crossings, in accordance with the analysis of the previous section [9].

Synchronous and induction machines. Rotating machines connected to the feeder, including large industrial synchronous generators and induction motors, contribute to the short-circuit current as the flux trapped in their windings decays. For synchronous machines, the contribution decays from a subtransient peak (several times the rated current) through transient and steady-state regimes with time constants of tens of milliseconds to seconds. For induction motors, the contribution decays more rapidly, typically within a few cycles, but can still be significant in plants with large installed motor capacity. These machine contributions add to the upstream fault current and must be considered in the breaker sizing [9, 15].

Inverter-interfaced resources. Voltage-source converters used to interface PV systems, wind turbines, battery storage and increasingly EV-to-grid services to the AC grid are typically rated only marginally above their nominal current. The control algorithm explicitly limits the output current to a maximum value, typically 1.1–1.5 p.u. of the rated current, in order to protect the semiconductor switches from damage. Depending on the control mode—grid following, grid forming or grid supporting—the converter response may take several forms [15, 18]:

- **Grid-following converters** synchronize to the grid voltage, typically through a phase-locked loop, and inject a current of controlled magnitude and phase angle. During a fault, they reduce their active current and may inject a controlled reactive current proportional to the voltage drop. If the voltage drop is severe, the converter rides through the fault for a limited time and disconnects if the fault persists.
- **Grid-forming converters** behave as controlled voltage sources and may attempt to maintain the voltage at their terminals. Their fault current contribution is therefore determined primarily by the source impedance and the maximum allowed current of the switches, similarly to a synchronous machine with very low inertia and a hard saturation limit.
- **Grid-supporting converters** combine features of the two above, providing droop-based voltage and frequency support during normal operation and switching to a current-limiting mode during severe faults.

Storage and DC links. Battery energy storage systems contribute to an AC fault through their inverter while it remains enabled, with the response governed by its control and current limits [15, 18]. A different mechanism applies to a DC-bus fault in a conventional grid-connected two-level voltage-source converter: its antiparallel diodes may form an uncontrolled rectifier path from the AC grid to the DC fault even after the gates are blocked. This must not be confused with an unrestricted DC-to-AC

diode path after blocking; the available paths depend on converter topology and fault location [18, 20].

Capacitor banks and DC-link capacitors. Capacitor banks installed for power-factor correction or harmonic filtering, as well as the DC-link capacitors of converters, can deliver very high but short-lived fault-current pulses. These pulses are limited only by the parasitic inductance of the wiring and may reach tens of kA for a few tens of microseconds. Their main effect on the protection device is to impose very high $\mathrm{d}i/\mathrm{d}t$ stress at fault inception [9, 20].

In a passive feeder dominated by a stiff grid and rotating machines, the above contributions add up to a well-defined and large fault current, with clear zero crossings and a predictable waveform. In a converter-dominated feeder, however, this convenient picture is much less reliable. Several phenomena combine to undermine the assumptions on which conventional overcurrent protection is built: the magnitude of the fault current may be only slightly higher than the rated current of the source, its waveform may be heavily distorted by the converter's current-limiting control, its angle may differ from that of a synchronous machine, and the time available before the converters shut down may be only a few milliseconds. The protection device must therefore be able to detect and clear such faults much faster than was acceptable in the past [8, 15].

3.3 Requirements for a modern AC protection system

The discussion of the previous sections suggests that a protection system intended for use in modern AC distribution systems should ideally combine the following properties [2, 8]:

- **Fast operation.** The total fault-clearing time, including detection, decision and interruption, should be on the order of a few milliseconds or less, so as not to exceed the short-circuit withstand capability of power-electronic loads and inverter-based sources, and to minimize the let-through energy delivered to the faulted equipment.
- **High sensitivity.** The device must be able to detect fault currents that are only slightly higher than the rated current, taking advantage of additional information such as voltage waveform distortion, current rate of rise, or communications with other devices in the network.
- **Bidirectional capability.** Because power can flow in either direction along a feeder—due to distributed generation, storage, regenerative drives or vehicle-to-grid systems—the breaker must be able to interrupt currents in both directions and to withstand voltages of both polarities.
- **Selectivity and coordination.** Despite the speed requirement, the device must coordinate with other protection devices upstream and downstream so that only the smallest possible portion of the network is disconnected for each fault [8, 9].

- **Discrimination against inrush and transient phenomena.** Motor starting, transformer energization, capacitor-bank switching and EV-charger inrush produce transient currents that should not cause nuisance tripping. Waveform-based criteria can supplement current thresholds. For example, transformer differential relays use harmonic restraint or blocking to discriminate magnetizing inrush from internal faults [21]. An SSCB implementation must account for the measurement window and decision latency of any such criterion.
- **High reliability and long lifetime.** Modern AC systems may require very frequent reconfiguration operations, especially in microgrids and at the interface with distributed generation, so the breaker must be capable of millions of operations without significant aging or maintenance.
- **Low conduction losses.** Because the breaker is continuously carrying load current, its on-state losses directly affect the efficiency of the protected system and the cost of the cooling system.
- **Compatibility with digital protection and communications.** The breaker should be able to report its status, receive trip and reset commands remotely, and integrate with substation automation systems based on IEC 61850 and similar standards.

As Chapter 4 shows, no existing technology fully satisfies all of these requirements. Electromechanical breakers are efficient and inexpensive but too slow; solid-state breakers are fast and controllable but have non-negligible conduction losses; hybrid breakers attempt to combine the best of both worlds at the price of additional complexity. The most promising solution for any given application therefore depends on the relative weight of the different requirements in that application, and this is one of the main themes of the chapters that follow.

Chapter 4

Circuit Breaker Technologies — A Review

This chapter presents a structured overview of the four main families of AC circuit breakers currently available or under active development: electromechanical breakers, hybrid breakers, resonant (forced-commutation) breakers and solid-state breakers. For each family the working principle, the main components, the typical performance figures, and the most important advantages and limitations are discussed. A comparative summary closes the chapter [2, 22].

4.1 Electromechanical circuit breakers

Electromechanical circuit breakers, often abbreviated as EMCBs and sometimes referred to as conventional or molded-case breakers depending on the voltage and current rating, dominate the market in essentially all voltage classes from low voltage up to extra-high voltage. They are based on a pair of metallic contacts that are mechanically separated when a fault is detected, and on an arc-extinction medium that assists the interruption of the current, in the simplest case at the next natural zero crossing (Figure 4.1). In practice the arc may reignite at that zero and be extinguished only once the arc voltage has risen far enough, as the measurement on a single pole of a contactor in Section 8.2.5 illustrates.

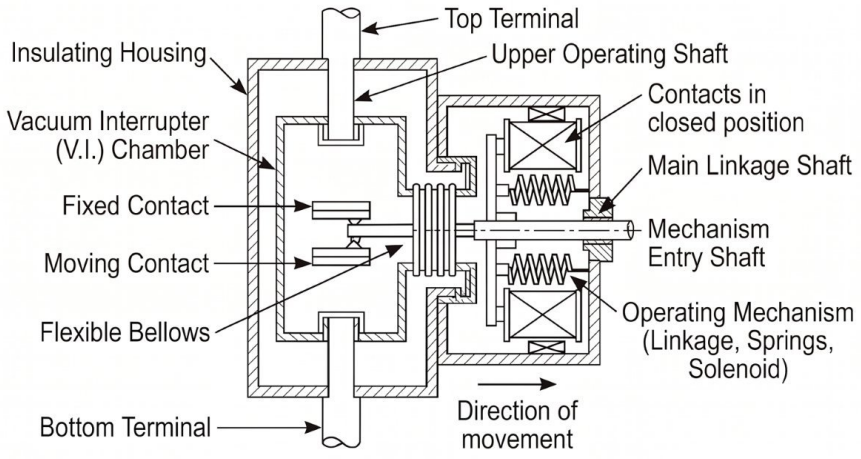


Figure 4.1. Schematic representation of a vacuum electromechanical circuit breaker, showing the fixed and moving contacts inside a vacuum chamber, the operating mechanism and the housing.

4.1.1 Operating principle and arc extinction

Under normal operating conditions the contacts of the breaker are closed and the current flows through them with very low resistance, typically below 1 mΩ. The contacts are held in the closed position either by mechanical springs or by latching mechanisms, sometimes assisted by an electromagnetic solenoid. When a fault is detected by an external protection relay (or by a built-in thermal-magnetic element in molded-case breakers), the operating mechanism receives a trip command and rapidly separates the contacts [9].

As the contacts move apart, the strong electric field at their surface, combined with the inductive nature of the circuit, ionizes the medium between them and an electric arc is established. The current keeps flowing through the arc, which dissipates energy primarily as heat and light. The interruption of the current is achieved by ensuring that, when the AC waveform reaches its next natural zero crossing, the arc is sufficiently de-ionized to prevent it from re-striking under the recovery voltage that appears across the contacts. The medium surrounding the contacts therefore plays a fundamental role in determining the performance of the breaker [22]. The most common technologies are:

- Air-magnetic breakers, in which the arc is cooled and stretched by a magnetic field applied perpendicular to its axis. These breakers are inexpensive but bulky and limited to low and medium voltages.
- Oil breakers, in which the arc forms inside mineral oil. The arc decomposes a small amount of oil, producing a gas pocket that extinguishes the arc. Oil breakers have largely been replaced by other technologies due to environmental and fire-safety concerns.
- SF6 breakers, in which the contacts open inside a chamber filled with pressurized sulfur hexafluoride. SF6 has excellent insulating and arc-quenching properties, but it is also a powerful greenhouse gas, which has led to international restrictions on its use.
- Vacuum breakers, in which the contacts are enclosed in a sealed vacuum chamber. In the absence of a gaseous medium, the arc is sustained by metallic vapor evaporated from the contacts themselves and is extinguished quickly at current zero. Vacuum breakers are now the dominant technology for medium-voltage applications because they combine excellent performance with the absence of any environmentally harmful medium.

4.1.2 Advantages and limitations

Electromechanical breakers are the result of more than a century of incremental development and represent a mature technology. Their main advantages are:

- Extremely low conduction losses, which are essentially limited by the metallic resistance of the closed contacts and busbars.
- High voltage and current scalability, with commercial products available for any rating from a few amperes at low voltage up to several kiloamperes at hundreds

of kilovolts.

- Galvanic isolation between the two sides of the breaker when it is in the open state.
- Maturity, low cost, and a well-developed ecosystem of standards, protective relays and accessories.

On the other hand, the technology has some intrinsic limitations:

- Typical operating times in the range of 30–80 ms, dominated by the mechanical movement of the contacts and the time required to reach the next current zero crossing. This is several orders of magnitude longer than the response time of power-electronic converters.
- Production of an electric arc that gradually erodes the contacts and limits the number of fault interruptions that the breaker can perform before maintenance or replacement. Typical figures are in the range of 10,000 mechanical operations and a few dozen interruptions at the rated short-circuit breaking current.
- Generation of electromagnetic noise and pressure waves during arc-quenching, which may be unacceptable in some applications.
- Need for periodic maintenance, including inspection of the contacts and possibly replacement of gases or oils.
- Reduced effectiveness in applications where the current does not have well-defined zero crossings, in particular DC systems [9].

4.2 Hybrid circuit breakers

Hybrid circuit breakers (HCBs) attempt to combine the low conduction losses of mechanical breakers with the fast response of semiconductor switches. In the most common architecture, a fast mechanical switch (typically a vacuum switch operated by a Thomson-coil actuator) [23] is placed in series with a small number of semiconductor switches, while a parallel branch containing a larger group of semiconductors is used to carry the current during the interruption transient. A third parallel branch, containing a metal-oxide varistor (MOV), is used to absorb the magnetic energy stored in the network inductance once the semiconductor branch has turned off [24]. The arrangement is shown in Figure 4.2.

During normal operation, the current flows almost exclusively through the mechanical branch, ensuring very low conduction losses. When a fault is detected, the main semiconductor switches of the commutation branch are first turned on, providing a low-impedance parallel path. The auxiliary semiconductor switch in the mechanical branch is then turned off, forcing the current to commutate to the parallel path. The fast mechanical switch can now open without any current flowing through it, so no arc is formed. Once the mechanical switch has reached a sufficient open distance, the main semiconductor switches are turned off and the current is forced into the MOV, which absorbs the energy stored in the network inductance and drives the current to

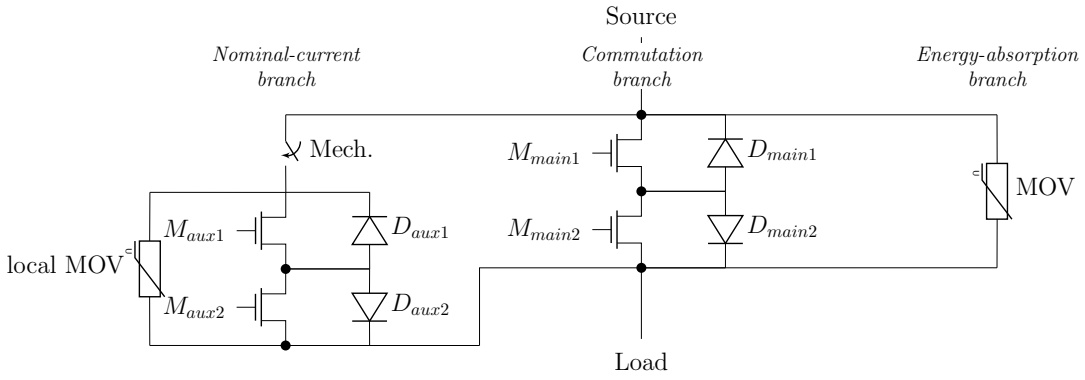


Figure 4.2. Generic architecture of a hybrid circuit breaker, showing the nominal-current branch with the fast mechanical switch and the auxiliary semiconductor switch, the parallel commutation branch with the main semiconductor switches, and the energy-absorption branch with the MOV.

zero [2, 24].

Hybrid breakers can achieve clearing times of a few milliseconds while keeping the conduction losses at a small fraction of those of a pure solid-state breaker. The main drawbacks are the increased complexity of the device (with several semiconductors, a fast mechanical switch and a dedicated control system) and the corresponding cost. Hybrid breakers were originally developed for HVDC applications, where pure solid-state breakers would be prohibitively expensive due to the very high number of semiconductors required, but the same architecture has more recently been proposed for AC medium-voltage applications as well [2, 23, 24].

4.3 Resonant (forced-commutation) circuit breakers

A distinct family of breakers occupies the conceptual space between the hybrid and the fully solid-state devices: the resonant, or forced-commutation, circuit breaker. Its central idea is to keep a robust, low-loss *semi-controlled* switch—almost invariably a thyristor (SCR)—as the main current-carrying element, and to add an auxiliary *LC resonant circuit* whose only purpose is to create, on command, an artificial zero crossing of the current through that switch. Thyristors are attractive as the main switch because they combine a very low on-state voltage drop, a high surge-current capability and a low cost per ampere; their well-known drawback is that they cannot be turned off through the gate and instead require the anode current to fall below the holding value before they recover their blocking state [25]. In an AC system this would normally mean waiting for the natural zero crossing of the line current—precisely the limitation that makes mechanical interruption slow. The resonant circuit removes this dependence by *forcing* a current zero whenever it is needed, as illustrated in Figure 4.3.

4.3.1 Operating principle

The interruption proceeds through a short sequence of phases:

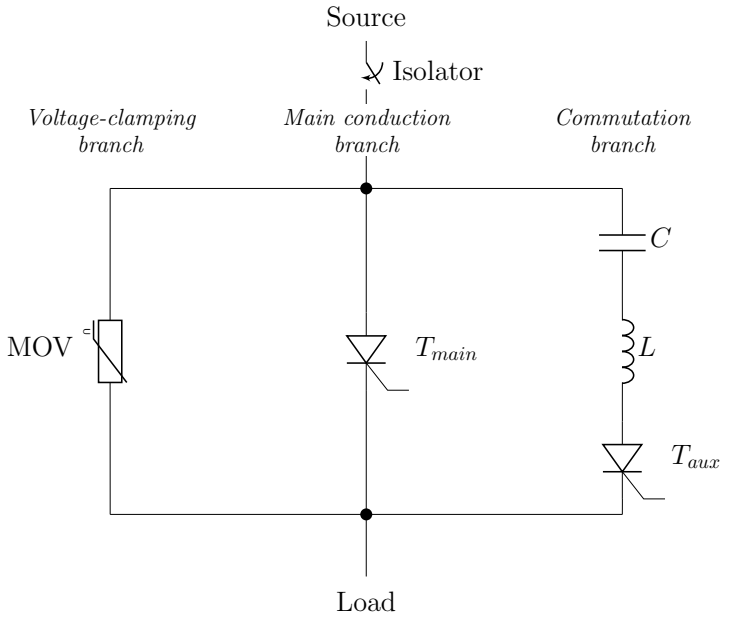


Figure 4.3. Architecture of a resonant circuit breaker, showing the main thyristor switch carrying the load current, the auxiliary commutation branch (precharged capacitor, resonant inductor and auxiliary thyristor) that injects the counter-current, the voltage-clamping (MOV) branch and the series mechanical isolator.

- **Normal conduction.** The load current flows through the main thyristor—in an AC breaker, through an anti-parallel pair of thyristors or through a single thyristor inside a diode bridge—with conduction losses limited to a single 1.2–2.0 V drop in the anti-parallel arrangement, or to three device drops in the diode-bridge arrangement. The commutation capacitor is kept precharged to a known polarity.
- **Current injection.** When a trip is required, the auxiliary thyristor is fired and the precharged capacitor discharges through the resonant inductor. The *LC* pair produces a half-sinusoidal current pulse, whose peak is by design larger than the current to be interrupted, injected in opposition to the main current.
- **Artificial current zero.** As the injected counter-current grows, the net current through the main thyristor falls and momentarily reaches zero. With the current below its holding value and a brief reverse bias applied by the capacitor, the main thyristor recovers its forward-blocking capability and turns off, without any natural zero crossing being required.
- **Energy absorption and isolation.** Once the main switch blocks, the network inductance drives the voltage up until the parallel MOV conducts and absorbs the stored magnetic energy, exactly as in a solid-state breaker. A series mechanical isolator can then be opened at zero current to provide galvanic isolation.

The peak and the duration of the injected pulse are fixed by the resonant values L and C and by the capacitor pre-charge voltage; these are chosen so that the counter-current exceeds the maximum prospective fault current and so that the resulting reverse-recovery interval is long enough for the thyristor to regain its blocking capability. In

AC applications the polarity of the injection must match the half-cycle in which the interruption occurs, which is why practical realizations adopt bidirectional arrangements (anti-parallel thyristors with a reversible commutation capacitor, or a diode bridge feeding a single thyristor) so that a current zero can be forced in either direction of the line current [22, 25].

4.3.2 Advantages and limitations

Resonant breakers were among the earliest attempts to obtain near-electronic interruption speeds using the rugged, inexpensive devices available before fully-controllable high-power transistors became practical, and the same principle underlies several modern thyristor-based SSCB topologies (anti-parallel SCR with auxiliary commutation, Z-source and T-source breakers) discussed in Chapter 6. Their main advantages are:

- Very low conduction losses and high surge-current capability, inherited directly from the thyristor main switch and markedly better than those of transistor-based solid-state breakers of the same rating.
- Interruption that does not have to wait for the natural zero crossing, giving clearing times well below those of a mechanical breaker (typically a fraction of a millisecond) while using only low-cost, highly robust semiconductors.
- A simple and very reliable main switch, with the active turn-off function delegated to an auxiliary branch that does not carry the load current continuously.

The principal limitations are:

- The need for an auxiliary commutation circuit—a precharged capacitor, a resonant inductor, an auxiliary thyristor and a charging supply—which adds volume and cost and must be dimensioned for the maximum prospective fault current.
- A reaction time still longer than that of a transistor-based solid-state breaker (tens to hundreds of microseconds rather than a few microseconds), because the artificial zero is produced by an LC oscillation of finite period rather than by a direct gate turn-off.
- A residual dependence on the correct precharge polarity and timing, which complicates the control compared with a simple gate-off command, particularly in AC where the required polarity changes every half-cycle.
- No active current-limiting or modulating capability. Once the auxiliary branch fires, the resonant breaker performs a single, all-or-nothing interruption dictated by the LC oscillation; it cannot regulate the current it carries. A transistor-based SSCB, by contrast, can use its controllable gate drive to hold the current within a prescribed band—switching the main device on and off, or operating it in a linear current-limiting mode—for a short interval. This allows the SSCB to ride through transient overcurrents and to discriminate a genuine fault from an inrush or load transient before committing to a trip, a fault-identification strategy that the thyristor main switch, lacking gate turn-off, cannot reproduce.

These trade-offs place the resonant breaker between the hybrid breaker, which relies on a moving contact for the actual interruption, and the fully solid-state breaker discussed in the next section, which dispenses with both the moving contact and the resonant circuit at the price of higher conduction losses.

4.4 Solid-state circuit breakers

Solid-state circuit breakers (SSCBs) replace the moving contacts of conventional breakers entirely with controllable semiconductor switches. The interruption of the current is no longer based on the mechanical separation of contacts and on the natural zero crossing of the AC waveform, but is instead achieved by turning off the semiconductor switches in a fraction of a microsecond. The absence of moving parts and arcing gives the device a unique combination of properties that are highly attractive across essentially every class of modern AC application [2, 6]:

- **Ultra-fast interruption.** The semiconductor turn-off itself takes a fraction of a microsecond, while the complete interruption – including detection, gate withdrawal and the clamping interval during which the network inductance is de-energized – is typically completed within some tens to a few hundred microseconds, several orders of magnitude faster than electromechanical breakers. This reduces the let-through energy and the voltage-sag depth seen by downstream loads by orders of magnitude.
- **Arc-free operation.** The interruption takes place inside the semiconductor without the formation of an electric arc. Contact erosion, mechanical noise, ionized-gas emissions and pressure waves are eliminated. This makes the device intrinsically suitable for explosive or sealed environments and for crowded enclosures where the acoustic and electromagnetic disturbances of a conventional breaker would be unacceptable.
- **Full controllability.** The on/off state of the device is commanded electronically by a digital signal. The breaker can therefore act simultaneously as a circuit breaker, a current limiter and a remotely operated switch; it can implement adjustable current-time tripping characteristics; and it can be integrated seamlessly into IEC 61850-based substation automation, accepting remote trip and reset commands, reporting its own status and coordinating with other protection devices through fast communication links.
- **Longevity.** The number of operations is limited only by the thermal cycling of the semiconductor packages, which typically allows more than 10^6 switching events—two to three orders of magnitude above the 10^3–10^4 operations of an electromechanical breaker. The absence of contact wear and of arc-quenching media also removes the need for periodic maintenance, which is particularly valuable in remote or hard-to-access installations.
- **No moving parts and silent operation.** The breaker has no mechanical linkage and produces no audible noise during operation. This is decisive in noise-sensitive

environments, on board ships and aircraft where vibration and mechanical wear are particularly damaging, and in compact enclosures where the mechanical clearance required by a conventional breaker is unavailable.

- **Compact and lightweight design.** The elimination of arc-quenching chambers, contacts and operating mechanisms, together with the increasing power density of modern wide-bandgap semiconductors, results in devices that are typically much smaller and lighter than electromechanical breakers of equivalent rating. This is essential in transportation, aerospace and naval applications.
- **Contribution to system stability and power quality.** Fast fault clearing limits the duration and depth of voltage sags propagated to the rest of the network. In converter-dominated systems, in particular, it allows converters to ride through the fault rather than disconnect, preserving generation and contributing to frequency stability [26, 27]. The same speed allows fast and selective fault location, which further reduces the affected area.
- **Inherent current-limiting capability.** Because the device can be commanded to turn off at any instant, it can implement active current limiting: as soon as the current exceeds a programmed threshold, the SSCB modulates its on-state or transfers the current to a dedicated limiting path, effectively imposing an upper bound on the fault current that the rest of the network sees. The same gate-level control allows the breaker to hold the current within a prescribed band for a short interval rather than committing immediately to a trip, so that a genuine fault can be discriminated from an inrush or load transient before the device interrupts. This reduces the short-circuit stress on transformers, cables, busbars and downstream switchgear, and may allow the use of equipment with lower short-circuit ratings [28].
- **Suitability for fast reclosing and autonomous reconfiguration.** The absence of arc-related aging and the very short tripping time make rapid reclosing schemes feasible: the breaker can perform several test operations within a fraction of a second, which is valuable wherever there is no arc path to de-ionize, such as in microgrid reconfiguration; on overhead lines the dead time remains dictated by arc de-ionization rather than by the breaker and for the autonomous reconfiguration of microgrids following a disturbance.
- **Environmental friendliness.** The technology requires no SF_6, mineral oil or other environmentally harmful insulating media, in line with the international restrictions that are progressively being imposed on the use of such substances.

The price for these advantages is paid mainly in conduction losses. The on-state voltage drop of a single IGBT or SiC MOSFET is typically in the range of 1–3 V, which produces continuous losses that can become significant for currents of several hundreds of amperes. In a 400 V / 600 A SSCB based on Si IGBTs, for example, the steady-state losses can easily reach 1 kW per pole, requiring an active cooling system. This is a much larger figure than for an electromechanical breaker of the same rating, and it directly affects the economic viability of the technology. The choice of the power semiconductor

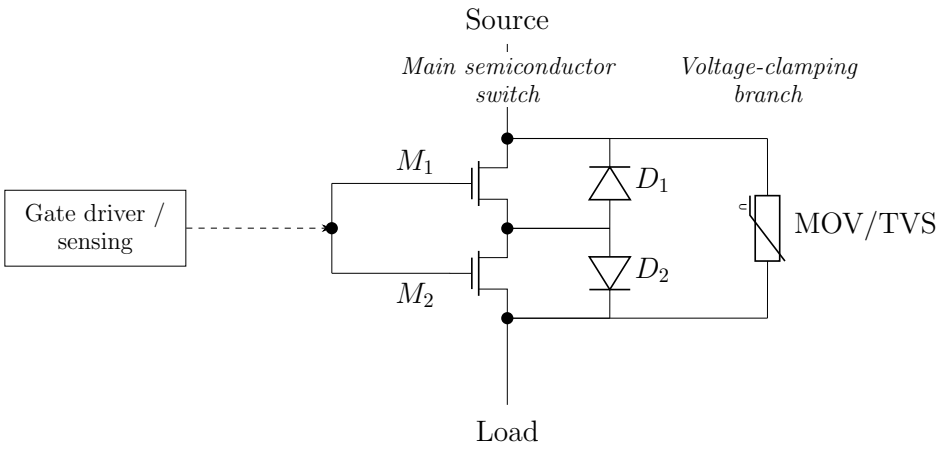


Figure 4.4. Generic architecture of a solid-state circuit breaker, showing the main semiconductor switch, the voltage-clamping (MOV/TVS) branch and the gate driver / sensing block.

device—and in particular the migration from silicon to wide-bandgap devices—is therefore one of the central design decisions for any SSCB, and is discussed in detail in Chapter 5 [2, 6].

Additional considerations for SSCBs include the need to absorb the magnetic energy stored in the network inductance when the current is interrupted, the protection of the semiconductors against the resulting overvoltage, the design of fast and accurate fault-detection circuits, and the management of bidirectional power flow in AC applications. All of these aspects are discussed in detail in the following chapters [2, 20].

4.5 Comparative discussion

Table 4.1 summarizes the main characteristics of the four families of circuit breakers reviewed in this chapter. The comparison is qualitative and indicative; precise figures depend strongly on the rated voltage, the rated current, and the specific implementation of each technology [2, 22, 24].

Table 4.1. Qualitative comparison of circuit-breaker technologies

Characteristic	Electro-mech.	Hybrid	Resonant	Solid-state
Interruption time	30–80 ms	2–5 ms	0.1–1 ms	1–100 μs
Conduction losses	Very low	Low	Very low	Moderate–high
Arc generation	Yes (managed)	Minimal	None	None
Lifetime (operations)	10^3–10^4	10^4–10^5	$> 10^5$	$> 10^6$
Galvanic isolation	Yes	Yes	Yes (isolator)	Requires aux. switch
Maintenance	Periodic	Reduced	Low	Minimal
Cost (relative)	Low	Medium–high	Medium	High
Maturity	Mature	Emerging	Established	Emerging (LV comm.)
Converter-based grids	Limited	Good	Good	Excellent

Several conclusions can be drawn from the comparison. Electromechanical breakers remain the most economical and most efficient solution in terms of conduction losses, but their relatively slow response makes them increasingly inadequate for the protection

of converter-dominated systems. Hybrid breakers occupy an intermediate position, offering a substantial improvement in speed while retaining most of the efficiency of mechanical breakers, at the cost of a more complex device. Resonant (forced-commutation) breakers chart a middle path of their own: by keeping a low-loss thyristor as the main switch they preserve the efficiency of mechanical interruption while reaching sub-millisecond clearing times, at the price of an auxiliary commutation circuit and a speed that is still well short of a transistor-based device. Solid-state breakers are the fastest and most flexible solution, with millions of operations achievable without maintenance and with full controllability, but their conduction losses and cost are currently higher than those of competing technologies. The continuing improvement of wide-bandgap semiconductors is gradually closing this gap, and several manufacturers have started to introduce commercial low-voltage AC SSCBs aimed at applications such as data centers, battery storage systems, and electric vehicle charging infrastructure; ABB demonstrated a low-voltage SSCB concept as early as 2019 [11], and evaluation-grade commercial hardware is now available from semiconductor vendors [12].

Chapter 5

Power Semiconductor Devices for SSCBs

The power semiconductor device is at the very heart of every solid-state circuit breaker. It is the element that physically carries the load current during normal operation, interrupts it in a few microseconds when a fault is detected, and—together with the voltage-clamping branch—withstands the recovery voltage in the off-state. Because the breaker is permanently inserted in series with the protected line, its on-state losses, its rated voltage and current, its turn-off capability and its short-circuit withstand time all map directly onto fundamental design parameters of the SSCB, such as efficiency, footprint, cost and reliability.

Modern power electronics offers a wide catalog of devices, each of which represents a different compromise among these requirements. Silicon-based technologies, refined over more than fifty years, dominate the medium- and high-power range thanks to their maturity, robustness and cost-effectiveness. Wide-bandgap (WBG) technologies, in particular silicon carbide (SiC) and gallium nitride (GaN), are rapidly displacing silicon in low- and medium-voltage applications where superior switching speed and high-temperature operation matter most. This chapter examines the principal devices of each family, with particular emphasis on AC SSCB applications, and concludes with a comparative discussion intended to guide the selection of the most appropriate device for a given specification.

5.1 Classification of power semiconductor devices

Power semiconductor devices can be classified along several orthogonal axes, each of which has direct implications for SSCB design [25]:

- **By semiconductor material:** silicon (Si), silicon carbide (SiC), gallium nitride (GaN), and, more recently, gallium oxide (Ga_2O_3) and diamond. The material determines the maximum electric field that the device can withstand, the maximum operating temperature, the achievable switching speed, and the cost per ampere.
- **By the nature of charge transport:** unipolar devices (such as MOSFETs and JFETs) conduct only one type of carrier (electrons), while bipolar devices (such as thyristors, IGBTs and GTOs) rely on conductivity modulation through minority-carrier injection. Bipolar devices typically achieve lower on-state voltage drops at high currents, though stored-charge effects make their switching slower.
- **By controllability:** devices may be uncontrolled (diodes), semi-controlled (classical thyristors, which can be turned on but not off through the gate), or fully controlled (IGBTs, MOSFETs, GTOs, IGCTs, ETOs). For an SSCB, full gate control is essential because the breaker must be able to interrupt the current on command without relying on natural zero crossings.

- **By the polarity of the conduction:** most power semiconductors conduct current in only one direction, while a few specialized devices (e.g. TRIACs, anti-parallel SCR pairs, monolithic bidirectional GaN switches) are intrinsically bidirectional. In AC SSCBs, where current must be interrupted in both directions, this property strongly influences the topology choice.
- **By the normally-on or normally-off behavior:** most modern devices are normally-off, which is generally regarded as a safer default. SiC JFETs are an important exception: they can be designed as normally-on devices, which conduct without any gate drive power and are therefore attractive for SSCB applications where minimal standby consumption is desired.

From the standpoint of an AC SSCB, the device must in addition withstand the system voltage in both polarities during the off-state. With few exceptions, conventional unipolar and bipolar devices block voltage in only one direction; bidirectional blocking is therefore typically achieved at the topology level (back-to-back arrangements), as discussed in Chapter 6. In what follows, each device family is presented with its physical operating principle and its specific advantages and limitations for AC SSCB use.

5.2 Silicon-based devices

Silicon-based power semiconductors remain the dominant choice in medium- and high-power applications. Decades of process refinement have led to extremely high reliability, well-understood failure mechanisms, mature packaging technologies, and a competitive cost per ampere. For SSCB applications, the main silicon devices of interest are the classical thyristor (SCR), the gate turn-off thyristor (GTO), the insulated-gate bipolar transistor (IGBT), the integrated gate-commutated thyristor (IGCT), the emitter turn-off thyristor (ETO), and the power MOSFET.

5.2.1 Thyristors (SCRs)

The silicon-controlled rectifier (SCR), commonly referred to simply as a thyristor, is a four-layer (PNPN) bipolar device with three terminals: anode, cathode and gate. When a positive voltage is applied between anode and cathode and a short current pulse is injected into the gate, the device latches into a low-impedance state and continues to conduct even after the gate signal is removed. The conduction can only be interrupted by reducing the anode current below a holding threshold, typically by means of an external commutation circuit or by the natural zero crossing of an AC current [25, 29].

In SSCB applications, thyristors are normally used in pairs connected in anti-parallel, so that current can flow in both halves of the AC waveform. Because thyristors lack inherent turn-off capability, they are most often employed in topologies that exploit auxiliary commutation circuits (e.g. capacitor-based forced commutation, Z-source or T-source breakers) to create the artificial zero-current crossing required for turn-off.

Advantages: extremely high surge-current capability, low on-state voltage drop (typically around 1.0–1.5 V even at several kA), excellent ruggedness and reliability, very high rated voltages up to several kV per device, and low cost per ampere. These properties make SCRs attractive whenever the breaker has to withstand large transient overcurrents during the brief interval before turn-off.

Limitations: lack of inherent turn-off capability through the gate, requiring external commutation circuits that increase complexity, cost and conduction losses; relatively slow recovery; and limited suitability for switching at high frequency. In a pure SSCB context, the use of SCRs is therefore typically restricted to specialized topologies (Z-source, current-source, anti-parallel SCR with auxiliary commutation) where their high surge capability and low cost outweigh the added complexity.

5.2.2 Gate Turn-Off thyristors (GTO and ETO)

The gate turn-off thyristor (GTO) is a development of the classical SCR in which the gate–cathode structure has been modified so that a large negative gate-current pulse can extract enough carriers from the cathode region to switch the device off. GTOs were historically the first family of fully controllable high-power semiconductors and have been used extensively in railway traction, industrial drives and FACTS applications. In SSCB contexts, GTOs can be used directly to interrupt the load current without an auxiliary commutation network, although they require very substantial gate-drive power.

The emitter turn-off thyristor (ETO) is a more recent device that combines a GTO with a series MOSFET in a single package. The MOSFET diverts the cathode current to the gate terminal during turn-off, removing the need for the very large negative gate-current pulse that the bare GTO demands and improving the turn-off speed [25]. SiC-based ETOs have been demonstrated in 15 kV-class breakers and represent a promising option for medium-voltage SSCBs [13].

Advantages: high blocking voltage (up to 6–10 kV per device for silicon, even higher for SiC-ETO variants), large turn-off current capability, and—compared with SCRs—the ability to interrupt the current without external commutation. The ETO variant further offers low gate-drive power requirements and substantially faster switching than the bare GTO.

Limitations: large minimum on-time and off-time (typically tens of microseconds), high gate-drive power requirements for the bare GTO, sensitivity to $\mathrm{d}V/\mathrm{d}t$ at turn-off and to $\mathrm{d}i/\mathrm{d}t$ at turn-on, and the need for snubber circuits that limit the switching trajectory inside the safe operating area. In modern designs, GTOs have largely been supplanted by IGCTs (described in Section 5.2.4) which retain the low on-state voltage drop of the GTO while offering substantially improved switching behavior.

5.2.3 Insulated-Gate Bipolar Transistors (IGBT)

The insulated-gate bipolar transistor, introduced commercially in the mid-1980s, has become the workhorse of medium- and high-power electronics. It combines the high

input impedance and easy gate-drive of a MOSFET with the conductivity-modulated, low on-state voltage drop of a bipolar transistor. Structurally, an IGBT can be thought of as a wide-base PNP transistor whose base current is supplied by an n-channel MOSFET, with the MOSFET providing the gate control and the PNP providing the conductivity modulation. Modern silicon IGBTs are commercially available with rated voltages from 600 V up to 6.5 kV and rated currents up to several kA per module, often integrated with anti-parallel freewheeling diodes [30].

For SSCBs, the IGBT is the reference device for the medium-voltage and high-power range. Its voltage-controlled gate allows the use of low-power, isolated drivers, while its short-circuit withstand time of typically 5–10 μs leaves a comfortable margin for fault detection. Hybrid HVDC breakers commercially deployed by ABB and others rely on series-connected IGBT stacks rated for several hundred kilovolts [24].

Advantages: simple voltage-controlled gate drive with very low static power consumption, low conduction losses at high currents thanks to conductivity modulation, robust short-circuit behavior, wide commercial availability up to multi-kV / multi-kA ratings, mature packaging and well-developed application know-how, and a strong ecosystem of gate-drive and protection circuits.

Limitations: moderate switching speed limited by minority-carrier recombination (a few hundred hertz to a few kilohertz for high-voltage devices, and some tens of kilohertz for 600–1200 V trench devices), a tail-current at turn-off that increases switching losses, non-zero on-state voltage drop at low currents (typically around 1–2 V even at very low load) and limited operating temperature compared with WBG devices. For SSCB applications operating continuously near rated current, the constant on-state voltage drop is the main contributor to conduction losses, often requiring forced-air or even liquid cooling [25, 30].

5.2.4 Integrated Gate-Commutated Thyristors (IGCT)

The IGCT is a hard-driven, fully-controllable derivative of the GTO in which the gate-drive unit is integrated with the device in a coaxial low-inductance package. During turn-off, the entire cathode current is commutated to the gate in less than 1 μs, effectively converting the device into a transistor for the duration of the turn-off transient. This eliminates the need for a turn-off snubber and cuts the switching losses well below those of the GTO [31]. IGCTs are commercially available at voltage ratings from 4.5 kV to 10 kV and current ratings up to 5 kA, making them particularly attractive for medium-voltage SSCBs and for HVDC applications [24].

Reverse-blocking IGCTs (RB-IGCTs) additionally feature blocking capability in both directions, which makes them particularly attractive for AC SSCB topologies where bidirectional voltage blocking is required. Because a single RB-IGCT already blocks both polarities, an anti-parallel pair used as the main switch of a medium-voltage AC breaker avoids the doubled on-state voltage drop inherent to a back-to-back arrangement of unidirectional devices, giving it a clear conduction-loss advantage over an equivalent back-to-back IGBT realization [2, 25].

Advantages: an on-state voltage drop below 2 V even at several kA, excellent

hard-switching capability, high blocking voltage, robustness against fault currents, and the elimination of bulky turn-off snubbers thanks to the hard-driven gate. The RB variant offers intrinsic bidirectional voltage blocking, which is highly desirable in AC applications.

Limitations: complex and costly integrated gate drive that must supply very large gate currents during turn-off; relatively slow turn-on; minimum on-time and off-time of several tens of microseconds; significant cost per device; and limited commercial supply chain compared with IGBTs. Like all silicon bipolar devices, IGCTs also produce a tail-current at turn-off and exhibit limited operating temperature.

5.2.5 Power MOSFETs

The power MOSFET is a vertical, majority-carrier device controlled by an insulated gate. Because conduction relies exclusively on electrons (in the more common n-channel variant), there is no stored charge to remove during turn-off, allowing very fast switching transitions (in the order of tens of nanoseconds). The on-state behavior is resistive—the device exhibits an on-state resistance $R_{DS(\mathrm{on})}$ rather than a constant voltage drop—which means that conduction losses are proportional to the square of the current and are very low for currents below a few amperes [25].

Silicon power MOSFETs are essentially the dominant active switch in low-voltage SSCBs, particularly below 200 V. For AC applications, two devices are typically arranged back-to-back so that their body diodes face in opposite directions, providing bidirectional blocking. Their main limitation is the steep increase of $R_{DS(\mathrm{on})}$ with rated voltage—approximately as the 2.4–2.5 power of the breakdown voltage—which makes silicon MOSFETs economically uncompetitive above 500–600 V [32].

Advantages: switching transitions in tens of nanoseconds; voltage-controlled, low-power gate drive; absence of stored-charge tail current; resistive on-state behavior that yields extremely low conduction losses at low currents; low cost in mainstream low-voltage classes ($\leq$ 200 V); and excellent commercial availability [32].

Limitations: rapid growth of $R_{DS(\mathrm{on})}$ with breakdown voltage, which makes the device unattractive above approximately 600 V; relatively poor body-diode performance; thermal sensitivity of $R_{DS(\mathrm{on})}$; and limited surge-current capability compared with thyristors. For SSCBs operating at line voltages above 500 V, silicon MOSFETs are typically replaced by SiC MOSFETs (see Section 5.3.1).

5.3 Wide-bandgap devices

Wide-bandgap (WBG) semiconductors—principally silicon carbide (SiC) and gallium nitride (GaN)—have transformed the landscape of power electronics over the past 15 years. Their fundamental physical advantages over silicon stem from a much higher critical electric field (around ten times that of silicon), which allows much thinner drift regions, lower on-state resistance and faster switching for a given breakdown voltage. SiC also offers higher thermal conductivity, which simplifies thermal management,

while GaN supports lateral structures with extremely low parasitic capacitance and inductance, enabling very high switching frequencies [14].

For SSCB applications, WBG devices bring three concrete benefits: significantly lower conduction losses than silicon at moderate to high voltages, much faster turn-off (often below 100 ns), and the ability to operate at higher junction temperatures, which reduces cooling-system requirements. The remainder of this section reviews the main WBG devices currently available or under active development.

5.3.1 SiC MOSFETs

The SiC MOSFET is currently the most commercially mature WBG device. Modern SiC MOSFETs are available at voltage ratings from 650 V to 3.3 kV (with 6.5 kV and higher under development) and at currents up to several hundred amperes per discrete device. Compared with a Si MOSFET of the same rated voltage, a SiC MOSFET has an on-state resistance one to two orders of magnitude lower; compared with a Si IGBT, it offers significantly lower conduction losses at low and moderate currents (because $R_{DS(\mathrm{on})} \cdot I$ is linear, while $V_{CE(\mathrm{sat})}$ is essentially constant) and much faster turn-off [14].

SiC MOSFETs are particularly well suited to low- and medium-voltage AC SSCBs. Commercial low-voltage AC SSCB products from major manufacturers (e.g. ABB's 1 kV-class concept breaker, several products from second-source vendors targeted at data-center applications) typically employ SiC MOSFETs in back-to-back configuration as the main switch [11]. Several research prototypes further explore the extension of SiC MOSFET-based AC SSCBs towards higher current and voltage classes [33], while medium-voltage DC breaker demonstrations in the several-kV range have so far relied on other high-voltage switch technologies, such as a SiC ETO combined with a fast mechanical switch [13].

What the device buys the designer is a combination that no silicon part offers at the same time: an on-state resistance one to two orders of magnitude below that of a Si MOSFET of the same class, a turn-off completed in under 200 ns, a junction temperature limit near 200 °C that relaxes the cooling problem, a body diode whose reverse recovery is good enough to be used rather than bypassed, and a die small enough to keep the module compact. The cost per ampere, historically the objection to SiC, has been falling steadily with production volume, although it remains above that of a silicon IGBT of equivalent rating [14, 34].

The objections are of two kinds. The first is practical and will fade: fewer package options than mature silicon, and the price premium just mentioned. The second is intrinsic to the technology. Gate-oxide reliability remains the most scrutinized aspect of the SiC MOSFET, because the oxide field is roughly 2.5 times higher than in a silicon device, the SiC/SiO_2 conduction-band offset is smaller and the interface-trap density higher; the gate-source voltage must therefore be held within a narrower window than a silicon designer is used to. The very speed that makes the device attractive also works against it: the high $\mathrm{d}V/\mathrm{d}t$ at turn-off can drive a displacement current through the Miller capacitance and turn the device partially back on unless the gate loop is actively clamped. To these must be added the short circuit withstand time, which for a SiC

MOSFET is only 1–3 μs and which places a correspondingly tight requirement on the speed of the fault-detection chain [2, 14, 34].

5.3.2 SiC JFETs

The SiC junction field-effect transistor (JFET) is a vertical, majority-carrier device controlled by a reverse-biased PN junction at the gate. Unlike the MOSFET, the SiC JFET does not have a gate oxide, which makes it inherently more rugged and improves its long-term reliability. SiC JFETs can be designed either as normally-on devices (conducting when the gate-source voltage is zero) or as normally-off devices (requiring a positive gate-source voltage to conduct). The normally-on variant is particularly interesting for SSCB applications because it conducts without any gate-drive power during normal operation; this property is exploited in several self-powered SSCB concepts [35].

In a normally-on SSCB, the breaker remains in the on-state by default; a negative gate-source voltage is applied only when the device must be turned off. This is the exact opposite of the behavior of an IGBT or MOSFET, where a positive gate-source voltage is required to maintain conduction. The attraction of the normally-on JFET is not fail-safe behavior — on the contrary, losing gate-drive power leaves it conducting — but the fact that it requires no standby gate power to stay on and that the turn-off energy can be harvested from the fault itself, so that no external auxiliary supply is needed to trip. The price to pay is that a fail-safe mechanism is required at start-up to ensure that the device does not conduct uncontrollably before the gate driver is initialized, typically by cascading the JFET with a small low-voltage Si MOSFET either in a cascode configuration, in which the JFET gate is tied to the source of the MOSFET, or in a direct-drive configuration, in which the two gates are driven independently.

The absence of a gate oxide removes at a stroke the reliability concern that dominates the SiC MOSFET literature, and it lifts the usable junction temperature to around 250 °C. On-state resistance for the voltage class is comparable to that of a SiC MOSFET, and the structure is intrinsically rugged. Against this, the gate drive is harder: switching off a normally-on device requires a negative gate-source voltage held within tight limits, since the gate is a PN junction and will break down if driven too far. Commercial availability is narrower than for SiC MOSFETs, and bidirectional blocking still calls for the same anti-series arrangement that unipolar devices require [12, 35].

The experimental platform of Chapter 8 is built on exactly this device class, in its direct-drive rather than cascode form: the Combo JFET brings both the JFET gate and the MOSFET gate out as separate terminals. The extra degree of freedom is not academic. It allows the JFET gate to be over-driven so that the effective on-state resistance falls below what a fixed cascode connection would give, it decouples the switching speed from the low-voltage stage, and it makes the junction temperature observable through the gate-source voltage without a separate sensor. The device therefore behaves as a normally-off switch from the outside while retaining, inside, the properties that make the normally-on JFET attractive in the first place [12].

5.3.3 GaN HEMTs

The gallium nitride high-electron-mobility transistor (GaN HEMT) is a lateral, majority-carrier device based on a two-dimensional electron gas formed at the AlGaN/GaN heterojunction. The lateral geometry, the absence of stored minority charge, and the very low parasitic capacitance and inductance allow GaN HEMTs to switch extremely fast, with transition times below 10 ns and switching frequencies easily exceeding 1 MHz. Commercial GaN HEMTs are currently available with rated voltages up to about 650 V and rated currents up to a few tens of amperes per discrete device, with 900 V- and 1.2 kV-class parts now entering the market.

For SSCB applications, GaN HEMTs are particularly attractive in low-voltage ($\leq$ 600 V), low-to-medium-current applications where extreme switching speed and compactness dominate the specification: aerospace and avionic systems, data-center DC distribution, consumer-grade smart breakers, and EV on-board chargers. Monolithic bidirectional GaN switches—single devices that block voltage and conduct current in both directions—are a particularly promising development for AC SSCBs, since they can replace a back-to-back pair of conventional switches with a single component [2, 36].

Advantages: extremely fast switching (below 10 ns); very low gate-charge requirements; low parasitic inductance thanks to the lateral structure; low on-state resistance for the voltage class; and the possibility of monolithic bidirectional structures. The lateral geometry also facilitates monolithic integration of multiple devices on a single die, including integrated gate drivers.

Limitations: currently restricted to voltage classes below 650 V (with 1.2 kV under development); limited current rating compared with vertical devices; need for very careful gate-drive design due to the low gate-source voltage range (typically only $\pm$6 V); short-circuit withstand time of only a few hundred nanoseconds in many devices; cost per ampere still higher than for mature silicon devices; and a thermal-management challenge due to the lateral structure, which concentrates losses in a small volume.

Gate-drive limits must be taken from the chosen device rather than treated as a single universal GaN voltage range. For example, the CoolGaN GIT guide specifies a current-injection gate interface, with a small steady on-state gate current and transient charging and discharging pulses; negative off-state bias is used to improve immunity to false turn-on [37].

5.3.4 SiC bipolar devices

Beyond the SiC MOSFET and JFET, several bipolar SiC devices are under active development for very high voltage applications. Among these, the SiC IGBT and the SiC ETO have been demonstrated at voltage ratings of 10 kV and above, and the SiC GTO has been shown to operate up to 15 kV. These devices combine the conductivity-modulation benefits of bipolar operation with the wide-bandgap advantages of SiC, achieving on-state voltage drops comparable to those of silicon devices but at much higher voltage classes and with significantly faster switching.

In the SSCB context, SiC bipolar devices represent the long-term path towards true

medium-voltage (10–35 kV) and high-voltage (above 35 kV) solid-state breakers, in which the number of series devices needed to reach a given system voltage falls by a large factor compared with silicon-based stacks. Their main practical limitation today is the limited commercial availability and the high cost, both of which are expected to improve as the SiC material technology matures.

Advantages: blocking voltages of 10 kV and above in a single device; low on-state voltage drop thanks to conductivity modulation; faster switching than silicon bipolar devices of the same voltage class; and high-temperature operating capability.

Limitations: limited commercial availability today; high cost; demanding gate-drive requirements (similar in nature to those of silicon IGCTs and GTOs); and still-immature long-term reliability data, which is particularly important for a protective device that must be available for many years [6, 13].

5.4 Comparative overview and selection criteria

Figure 5.1 summarizes the approximate voltage and current operating ranges of the principal power semiconductor devices used in SSCB applications. The figure should be read with caution: device boundaries are continuously being pushed by research and industrial development, particularly for wide-bandgap devices, and the values shown here represent the bulk of commercially available products rather than absolute limits.

Beyond the raw voltage and current ratings, the choice of the power semiconductor device for a specific SSCB application is the result of a multi-criteria trade-off. The most important criteria can be summarized as follows:

- **Rated voltage and current.** The device must be able to block the full system voltage in the off-state, including an appropriate safety margin for transient overvoltages, and to conduct the rated load current in the on-state. For currents exceeding the rating of a single device, parallel connection is necessary, which raises issues of current sharing in steady state and during switching transients.
- **Conduction losses.** Because the SSCB carries the load current continuously, the on-state voltage drop is a dominant figure of merit. Bipolar devices (IGBT, IGCT, thyristor) offer essentially constant on-state voltage and are preferable at high currents, while unipolar devices (MOSFET, JFET, HEMT) offer resistive behavior that is advantageous at low and moderate currents.
- **Switching speed and turn-off capability.** The device must be able to turn off the maximum interrupted current quickly enough to keep the energy dissipated during the turn-off transient within safe limits. This typically rules out non-controllable devices such as classical SCRs unless they are combined with external commutation circuits.
- **Short-circuit withstand time.** During the interval between the fault inception and the actuation of the SSCB, the device must withstand the fault current without being destroyed. Si IGBTs typically withstand short circuits for 5–10 μs, SiC MOSFETs for 1–3 μs, and GaN HEMTs for less than 1 μs, which imposes increasingly

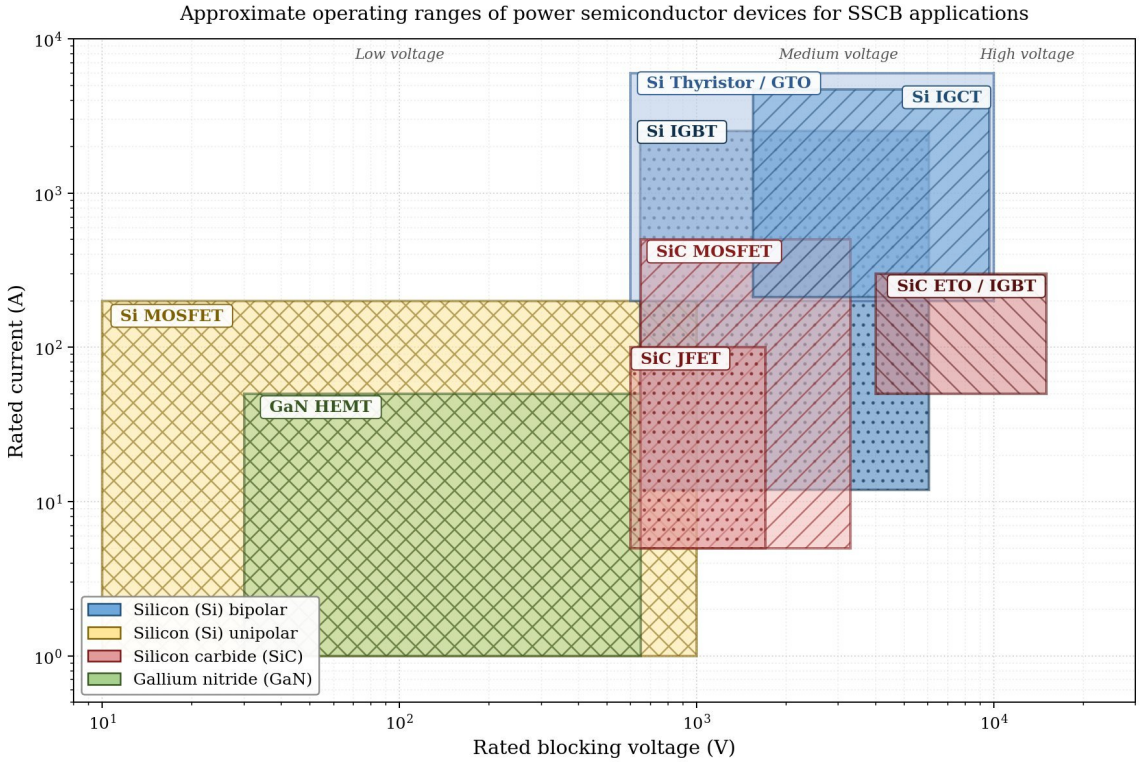


Figure 5.1. Approximate operating ranges (rated blocking voltage versus rated current) of the principal power semiconductor devices used in SSCB applications. Both axes are logarithmic. Silicon bipolar devices (top right) dominate the high-power region, silicon and wide-bandgap unipolar devices share the lower-power region, and emerging SiC bipolar devices (SiC ETO / IGBT) target the highest voltage class.

stringent requirements on the speed of the detection and gate-drive subsystems as the technology becomes faster.

- **Bidirectional capability.** In AC applications, the device must be able to block voltage and conduct current in both directions. Most devices are unidirectional in one or both senses, leading to the back-to-back arrangements discussed in Chapter 6; reverse-blocking IGCTs and emerging monolithic bidirectional GaN switches represent a more compact alternative.
- **Gate-drive complexity and power.** Voltage-controlled devices (MOSFET, IGBT) require very low gate-drive power, while current-controlled devices (GTO, classical IGCT) demand high gate currents during turn-off. For normally-on JFETs, special start-up provisions are required to keep the device in the off-state until the gate driver is ready.
- **Cost and availability.** The price per ampere of WBG devices is decreasing rapidly but is still higher than that of mature silicon devices. The total cost of an SSCB also includes the gate driver, the cooling system, the voltage-clamping branch and the housing, all of which depend on the choice of semiconductor.

Table 5.1 summarizes the principal characteristics of the devices reviewed in this chapter as a first-pass selection guide. As a rough rule of thumb, low-voltage ($\leq 1\,\mathrm{kV}$) AC SSCBs are dominated by SiC MOSFETs in back-to-back configuration, occasionally

Table 5.1. Comparative overview of power semiconductor devices for SSCB applications

Device	**Material**	V_{max}	I_{max}	**Gate control**	**Speed**	**Best suited for**
Silicon devices						
Thyristor (SCR)	Si	6 kV	5 kA	On only	Slow	High-surge AC, Z-source
GTO / ETO	Si / SiC	6–15 kV	3 kA	Full	Medium	High-voltage AC/DC, MVDC
IGBT	Si	6.5 kV	3 kA	Full	Medium–fast	MV AC/DC SSCBs, HVDC HCB
IGCT (RB-IGCT)	Si	10 kV	5 kA	Full	Medium	MV AC SSCBs, low losses
Power MOSFET	Si	1 kV	200 A	Full	Fast	LV AC SSCBs ($<$ 600 V)
Wide-bandgap devices						
SiC MOSFET	SiC	3.3 kV	500 A	Full	Very fast	LV/MV AC SSCBs, modern
SiC JFET	SiC	1.7 kV	100 A	Full (norm. on)	Very fast	Self-powered SSCBs
GaN HEMT	GaN	650 V	50 A	Full	Ultra fast	Aerospace, LV, compact
SiC ETO / IGBT	SiC	15 kV	300 A	Full	Fast	Future MV/HV SSCBs

supplemented by Si MOSFETs in the lowest-voltage classes; in the medium-voltage range (1–35 kV) Si IGBTs and Si IGCTs remain the standard choice, with SiC MOSFETs and SiC bipolar devices gaining ground as their cost decreases; and GaN HEMTs are restricted today to specialized low-voltage applications where their switching speed and compactness are worth the restricted voltage range.

The selection of the optimal device is ultimately application-specific. For the AC SSCBs targeted in this thesis—operating at line voltages typical of low-voltage distribution networks (230 V single-phase, 400 V three-phase)—a back-to-back configuration of SiC MOSFETs represents the most balanced compromise between speed, on-state losses, cost and commercial availability. This choice is the one adopted for the simulation studies of Chapter 7. The experimental platform of Chapter 8 instead uses a commercial Combo JFET board, in which a normally-on SiC JFET is placed in series with a low-voltage silicon MOSFET — an arrangement that trades the simplicity of a single normally-off device for a lower on-state resistance.

Chapter 6

Solid-State Circuit Breakers — Architecture and Topologies

Building on the device-level analysis of the previous chapter, this chapter examines the solid-state circuit breaker as a complete subsystem. The generic architecture is presented first, followed by a description of the typical voltage and current waveforms during fault interruption. The principal AC SSCB topologies are then discussed, together with the auxiliary subsystems (voltage clamping, gate driver, fault detection) that complete the design. The chapter closes with a review of the most representative SSCB applications.

6.1 Generic SSCB architecture

A solid-state circuit breaker can be described, at a sufficiently abstract level, as the combination of the four functional blocks shown in Figure 4.4 [10]:

- **Main semiconductor switch.** One or more controllable power-electronic devices arranged so as to be able to interrupt the load current when commanded to do so. In an AC breaker, the switch must be capable of blocking voltage and conducting current in both directions, which generally requires either a back-to-back arrangement of unipolar devices or the use of inherently bidirectional structures.
- **Voltage clamping / energy absorption branch.** A parallel branch, typically containing a metal-oxide varistor (MOV) or a transient-voltage-suppression (TVS) device, that absorbs the inductive energy of the network when the semiconductor switch is turned off and that limits the voltage across the switch to a safe value.
- **Gate driver.** The electronic interface between the control logic and the main switch, responsible for delivering the gate-current or gate-voltage pulses required to drive the device into the on-state and the off-state [38]. The gate driver also includes isolation barriers, auxiliary power supplies and protection features such as Miller-clamping and short-circuit detection.
- **Sensing and control system.** The combination of current and voltage sensors and digital or analog control circuits that monitors the operating state of the main circuit, identifies abnormal conditions, and generates the trip command to the gate driver. The control system may also implement communication with the supervisory protection system and coordinate with other breakers in the network.

A small number of additional optional elements are commonly found in practical SSCB designs. The most important is the mechanical isolator, a slow disconnect switch placed in series with the main semiconductor branch and operated only after the current has been interrupted. The isolator provides the galvanic isolation that the semiconductor

switches alone cannot guarantee in their off-state, due to the small but non-zero leakage current that always flows through them. Another common element is a fault-current-limiting inductor, which is occasionally inserted in series with the breaker to slow down the rate of rise of the fault current and to give the control system more time to react; however, the addition of such inductors increases the energy that the MOV must absorb at the end of the interruption and is therefore subject to a trade-off [22].

A further auxiliary element, closely related to the voltage-clamping branch but functionally distinct from it, is the snubber circuit connected directly across the main semiconductor switch. Whereas the MOV branch is dimensioned to absorb the bulk of the magnetic energy stored in the network inductance, the snubber has the more local task of limiting the rate of rise of the voltage ($\mathrm{d}v/\mathrm{d}t$) across the device and of damping the high-frequency oscillations excited by the parasitic inductance and capacitance of the commutation loop. Whether a snubber is actually *necessary* is not a universal property of the SSCB but depends strongly on the device technology chosen for the main switch [20, 22, 25, 31]:

- **Thyristor-type devices (SCR, GTO, IGCT).** The requirements differ between device families. Conventional SCRs often use an RC ($\mathrm{d}v/\mathrm{d}t$) snubber to prevent spurious re-triggering caused by a fast re-applied forward voltage, usually complemented by a series $\mathrm{d}i/\mathrm{d}t$-limiting inductor. Gate turn-off thyristors (GTOs) additionally need a bulky polarized RCD turn-off snubber to keep the device within its safe operating area during the turn-off transient, which is one of the main practical drawbacks of GTO-based designs. The hard, low-inductance gate drive of an IGCT allows operation without a turn-off snubber. Turn-on $\mathrm{d}i/\mathrm{d}t$ limitation and the device's voltage and switching limits must still be respected.
- **IGBTs.** Insulated-gate bipolar transistors can frequently be operated "snubberless" when driven by a modern gate driver that provides active clamping and a controlled turn-off speed. A small RCD clamp snubber is nevertheless often retained in high-power or series-connected designs, in order to limit the turn-off overvoltage produced by the stray inductance of the commutation loop and to assist in the static and dynamic voltage sharing between series devices.
- **MOSFETs, in particular wide-bandgap (SiC and GaN) devices.** Owing to their very fast switching and to the protection features built into their gate drivers (Miller clamp, active gate-voltage clamping), these devices are usually operated without a turn-off snubber. A small RC snubber is sometimes added solely to damp the voltage ringing and the associated electromagnetic interference produced by the high $\mathrm{d}v/\mathrm{d}t$, rather than to protect the device itself.

In all cases the snubber complements, but does not replace, the MOV-based energy-absorption branch: the two elements act on different time scales and absorb very different amounts of energy. The detailed design of both is treated together with the other auxiliary subsystems in Section 6.4.

6.2 Operating principle and typical waveforms

The operation of an SSCB during a fault can be divided into a small number of well-defined phases, which are best described with reference to the typical waveforms shown in Figure 6.1. The waveforms correspond to the single-phase AC test case analyzed in Chapter 7, in which a 230 V (RMS), 50 Hz source feeds an inductive load through the breaker. The defining feature of the AC case, with respect to the more familiar DC one, is that both the source voltage and the load current are sinusoidal: the instant at which the fault occurs and at which the breaker is commanded to open — the so-called *point on wave* — is therefore not fixed, and the severity of the interruption depends on the phase angle of the source voltage at that instant.

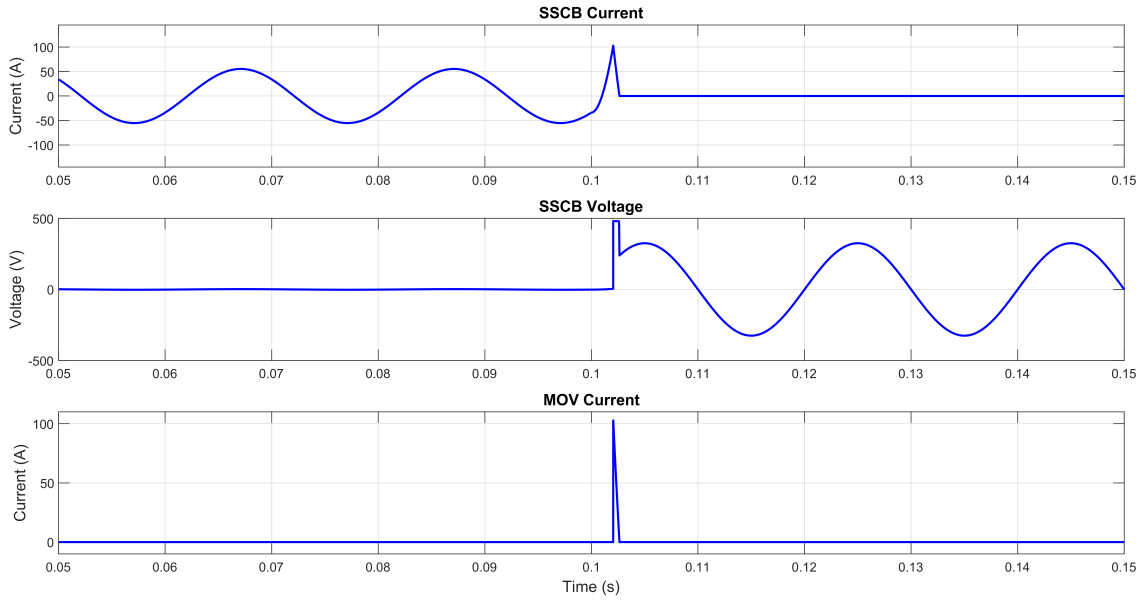


Figure 6.1. Typical waveforms of the current through the main switch (I_{sw}), the voltage across the breaker (V_{br}) and the current through the MOV (I_{mov}) during the interruption of a fault.

Phase 1: Normal operation. Under steady-state conditions the main semiconductor switch — or the bidirectional switch pair, in the AC case — is in the on-state. The current through the breaker is the sinusoidal load current, the voltage across the breaker is limited to the small on-state voltage drop of the conducting device(s) (typically a few volts), and the MOV operates in its leakage region with negligible current. The power dissipated in the breaker corresponds entirely to the conduction losses of the semiconductor, which in a bidirectional AC switch are incurred during both half-cycles of the line current [2].

Phase 2: Fault detection. When a short circuit occurs in the downstream system, the current through the breaker departs from its sinusoidal trajectory and starts to rise rapidly. The instantaneous rate of rise is governed by $\mathrm{d}i/\mathrm{d}t = \left(v_s(t) - v_{arc}\right)/L$, where $v_s(t)$ is the instantaneous source voltage, v_{arc} the fault arc voltage and L the loop inductance, and may easily reach hundreds or thousands of amperes per microsecond in low-inductance circuits. Because $v_s(t)$ is sinusoidal, the steepness of the fault current

depends on the point on wave: a fault occurring near the voltage peak produces the fastest rate of rise, and therefore the largest let-through current for a given detection threshold and trip delay, whereas a fault near a voltage zero develops more slowly but carries the largest DC offset and hence the highest prospective peak. The sensing system detects the abnormal condition either when the instantaneous current exceeds a fixed threshold (in the present work 100 A, i.e. somewhat above the ≈ 58 A peak of the normal load current) or when its rate of rise exceeds a predefined value. The detection time is determined primarily by the bandwidth of the current sensor and the speed of the comparator or digital processor used to evaluate the trip condition [2, 39].

Phase 3: Turn-off of the main switch. Once the trip condition is satisfied, the gate driver applies a turn-off command to the main semiconductor switch. A key distinction with respect to a conventional line-commutated device must be stressed here: a fully controllable SSCB does not wait for the natural zero crossing of the AC current, but forces the switch into the blocking state actively, at whatever point of the cycle the trip command is issued. The turn-off is completed in a few hundred nanoseconds to a few microseconds, depending on the device technology and on the magnitude of the current being interrupted. As the current through the switch decreases, the voltage across it rises rapidly, driven by the inductive voltage $L \cdot \mathrm{d}i/\mathrm{d}t$ of the network. Without a voltage-clamping device this voltage would easily exceed the breakdown voltage of the switch and destroy it; in Figure 6.1 it is instead limited to the clamping level of the MOV, appearing as the short voltage spike at the instant of interruption [2, 20].

Phase 4: Energy absorption. When the voltage across the breaker reaches the clamping level of the MOV, the varistor enters its conducting region and the current is diverted from the main semiconductor switch into the MOV branch (the short current pulse visible in the bottom trace of Figure 6.1). The MOV behaves approximately as a constant-voltage element, so the current through it is forced to zero at a rate $(V_{\mathrm{clamp}} - v_{\mathrm{s}}(t))/L$, where V_{clamp} is the clamping voltage of the MOV and $v_{\mathrm{s}}(t)$ the instantaneous source voltage. During this phase the MOV absorbs the magnetic energy stored in the network inductance, plus the energy supplied by the source until the current is fully extinguished. Treating the source voltage as approximately constant over the (very short) absorption interval, the energy absorbed by the MOV can be estimated by

$$W_{\mathrm{MOV}} \approx \frac{1}{2}\, L\, I_{\mathrm{max}}^{2}\, \frac{V_{\mathrm{clamp}}}{V_{\mathrm{clamp}} - |v_{\mathrm{s}}(t_0)|}, \tag{6.1}$$

where I_{max} is the maximum interrupted current and $v_{\mathrm{s}}(t_0)$ the source voltage at the instant of interruption. Equation (6.1) reduces to the familiar DC expression when $|v_{\mathrm{s}}(t_0)|$ is replaced by the constant DC voltage V_{dc}. For a given interrupted current, this approximation gives the highest absorbed energy when the source voltage is near its peak, $|v_{\mathrm{s}}(t_0)| \approx \hat{V}_{\mathrm{s}}$. The actual worst case must consider both the interrupted current and the point on wave; their maxima need not coincide. The MOV must be rated for the resulting energy requirement with adequate margin [20, 40]. As in the DC case, a higher clamping voltage produces a faster decay of the current and reduces the energy absorbed, but at the cost of a higher voltage stress on the semiconductor switch and on the surrounding equipment. A further constraint specific to the AC case is that the

clamping voltage must lie safely above the peak value of the source voltage, $V_{\text{clamp}} > \hat{V}_{\text{s}}$, so that the MOV does not conduct on every half-cycle during normal operation; a typical compromise places V_{clamp} at 1.5–2.2 times the peak system voltage [22].

Phase 5: Recovery and isolation. When the current through the MOV reaches the leakage level, the breaker has fully interrupted the fault. From this moment the open breaker must withstand the recovery voltage; in the AC case this is no longer a constant value but the full sinusoidal source voltage, which now appears across the blocking switch and oscillates between $\pm\hat{V}_{\text{s}}$ on every cycle. This is clearly visible in the center trace of Figure 6.1, where the voltage across the breaker becomes a 50 Hz sinusoid of amplitude equal to the source peak once the current has been extinguished. The blocking-voltage rating of the semiconductor and the clamping voltage of the MOV must both accommodate this recurring peak. The MOV itself returns to its high-resistance state and carries only its negligible leakage current. If galvanic isolation is required, a series mechanical isolator can now be opened with no current flowing through it. The breaker can be subsequently reclosed either by an automatic reclosing algorithm or by a manual command, once it has been verified that the downstream fault has been cleared.

6.3 Topologies of AC solid-state circuit breakers

The realization of an AC SSCB is complicated by the fact that the breaker must be capable of blocking voltage and conducting current in both directions. Several topologies have been proposed to achieve this, each with its own combination of advantages and limitations. The most representative are described below [2, 10].

Back-to-back (anti-series) configuration. Two unidirectional switches (typically MOSFETs or IGBTs) are connected in anti-series, with their internal body diodes (or external anti-parallel diodes) facing in opposite directions. This configuration is conceptually simple and is the most widely used in low-voltage AC SSCBs (Figure 6.2). In the on-state, the load current flows through the channel of one transistor and, since both devices are gated on, through the channel of the other in the reverse direction; in the off-state, one transistor blocks the positive half-cycle of the voltage and the other blocks the negative half-cycle. The main drawbacks are the doubled on-state voltage drop (the current always flows through two devices in series) and the need to coordinate the gate-drive of the two switches, which are at different reference potentials [2, 32].

Common-source / common-drain configurations. A practical variation of the back-to-back topology connects the sources (or the drains) of the two devices together, the common-source arrangement giving both devices the same gate reference and therefore allowing a single isolated gate-drive supply. The common-source arrangement is particularly popular because it places the two gate terminals at approximately the same potential, simplifying the gate driver. The common-drain arrangement is sometimes preferred when the package or the layout makes the drain connection easier [2, 25].

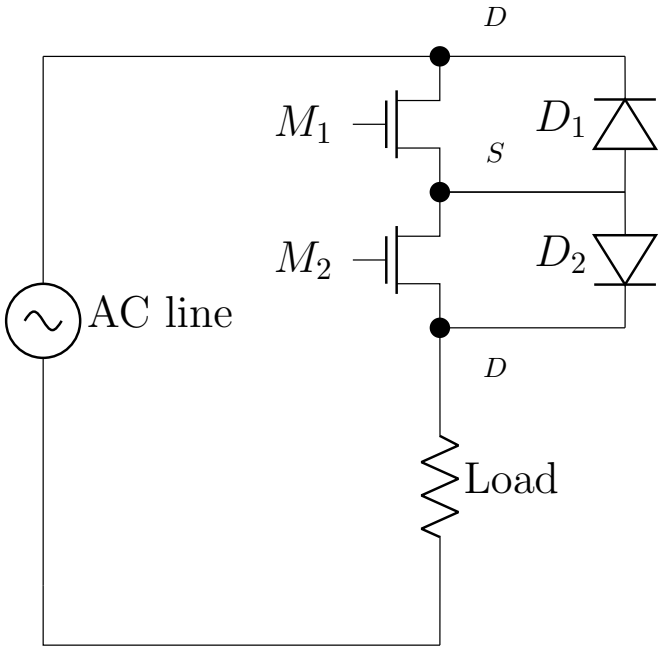


Figure 6.2. Back-to-back (anti-series) AC SSCB topology using two SiC MOSFETs. With both gates enabled, the MOSFET channels conduct in either current direction; with both gates disabled, the opposing body diodes allow the pair to block either voltage polarity.

Reverse-blocking devices. A more elegant solution is to use a single bidirectional or reverse-blocking power semiconductor device. Reverse-blocking IGBTs (RB-IGBTs) and reverse-blocking IGCTs (RB-IGCTs) can block voltage in both directions and are well suited for AC SSCB applications. Anti-parallel pairs of RB-IGCTs have been demonstrated in medium-voltage AC breakers with very low on-state voltage drop and reduced device count compared with conventional back-to-back arrangements. Bidirectional vertical MOSFET structures with reverse blocking capability are also under active development [2, 6].

Diode-bridge with single switch. In this topology, four diodes arranged in a full-bridge rectifier configuration are placed in front of a single unidirectional power switch (Figure 6.3) [2, p. 369]. The bridge converts the bidirectional AC current into a unidirectional current flowing through the switch, which can therefore be a simple MOSFET or IGBT. The advantage of this approach is that only one main switch and one gate driver are required, irrespective of the polarity of the system. The disadvantage is the additional conduction loss: the current passes through two bridge diodes and the main switch. The resulting loss depends on the diode forward voltages, the switch technology, current and temperature; counting device drops alone does not establish a fixed percentage penalty relative to a back-to-back arrangement [2, 32].

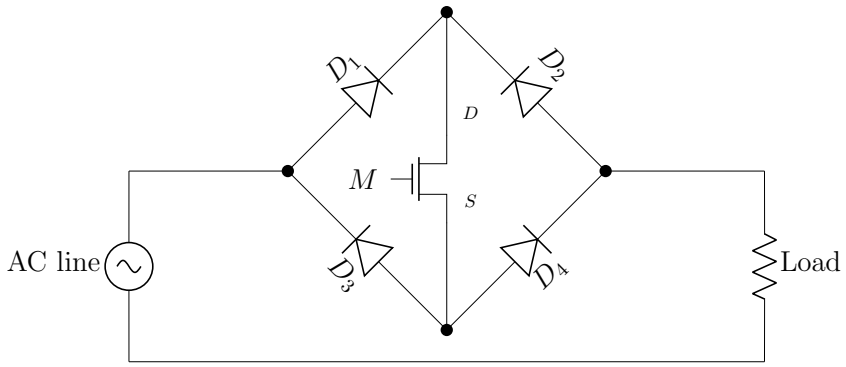


Figure 6.3. Diode-bridge AC SSCB topology, in which four rectifier diodes convert the AC current into a unidirectional current that is interrupted by a single power semiconductor switch.

Thyristor-based topologies (anti-parallel SCR, Z-source, T-source). An anti-parallel pair of silicon-controlled rectifiers can carry either polarity of AC current with only one SCR in the conducting path. Removing the gate signal does not turn an SCR off: the conducting device must be commutated below its holding current and allowed sufficient recovery time before forward voltage is reapplied [25, 29]. Figure 6.4 shows a simplified AC arrangement with a controlled resonant commutation branch. A precharged capacitor and an inductor generate a pulse that diverts current from the conducting SCR. The capacitor polarity must be selected for the actual line-current direction; the gate of the opposite SCR remains inhibited throughout the interruption. The auxiliary branch must subsequently cease conducting, allowing the MOV to absorb the remaining network energy.

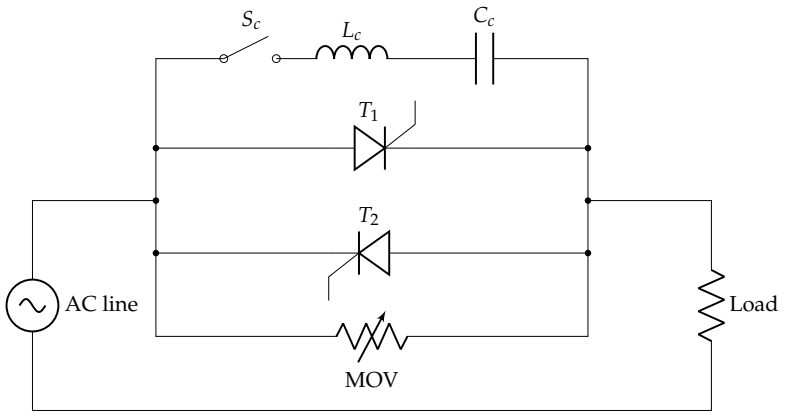


Figure 6.4. Anti-parallel-SCR AC breaker with a bidirectional commutation switch S_c, resonant components L_c, C_c, and MOV. Capacitor precharge and polarity selection, sensing and gate drivers are omitted; this is not a Z-source or T-source circuit.

Z-source and T-source (coupled-inductor) breakers are related thyristor-based families developed primarily for DC interruption. Their impedance networks create a current zero in the main SCR during a fault; coupled-inductor variants can improve the grounding arrangement and the normal-current path [19, 41]. These basic DC circuits must not be interpreted as directly interchangeable with the anti-parallel AC pair: AC

operation requires appropriate bidirectional commutation or rectification. Their appeal is the combination of surge-current capability and low on-state loss, at the expense of an additional commutation network.

Three-phase configurations. For three-phase AC systems, the simplest realization is to use one bidirectional SSCB per phase, with coordinated control between the three breakers. More compact topologies can be obtained by sharing some of the semiconductor devices among the three phases, or by combining the SSCB function with that of a static transfer switch [2].

6.4 Auxiliary circuits

6.4.1 Voltage clamping and snubber circuits

As discussed in Section 6.2, the inductive energy stored in the network must be absorbed by an auxiliary element when the main semiconductor switch is turned off, in order to keep the voltage across the switch within safe limits. Several types of voltage-clamping and snubber circuits are used in practice [20, 22]:

- **Metal-oxide varistors (MOVs).** MOVs are zinc-oxide-based devices that exhibit a highly non-linear voltage-current characteristic: they behave as an open circuit below their clamping voltage and as an approximately constant-voltage element above it. They can absorb very large amounts of energy and are the most common voltage-clamping element in medium- and high-power SSCBs; because of this central role they are treated separately and in more detail in Section 6.4.2.
- **Transient-voltage-suppression (TVS) diodes.** TVS diodes are reverse-biased PN junction diodes optimized to clamp transient overvoltages. They have faster response than MOVs but lower energy-absorption capability. They are therefore more suitable for low-power circuits, including gate drivers for series-connected devices.
- **RC, RCD and active snubbers.** When the rate of change of the voltage across the switch ($\mathrm{d}V/\mathrm{d}t$) must be limited—for example to reduce electromagnetic interference or to keep the displacement current of stray capacitances within safe limits—a small capacitor in parallel with the switch, possibly in series with a damping resistor and a freewheeling diode, can be added. Active snubbers using a small auxiliary switch can also be implemented when the highest performance is required.

The selection of the clamping voltage is the central design decision for the energy-absorption branch. A higher clamping voltage reduces the energy to be absorbed and the interruption time, but increases the voltage stress on the surrounding equipment. Typical values are between 1.5 and 2.2 times the peak system voltage [22].

6.4.2 The metal-oxide varistor

Because the metal-oxide varistor is, after the main semiconductor switch itself, the single most critical component of the breaker — it alone determines the voltage to which the network is allowed to rise during interruption and it alone absorbs the magnetic energy released by the network inductance — it deserves a more detailed treatment than the brief description given above.

Construction and conduction mechanism. A modern varistor is a ceramic block formed by sintering zinc-oxide (ZnO) powder together with small quantities of other metal-oxide additives (most importantly Bi_2O_3, together with oxides of antimony, cobalt, manganese and others). During sintering the material organizes itself into highly conductive ZnO grains, a few tens of micrometers across, separated by thin insulating intergranular layers. Each individual grain boundary behaves electrically as a pair of back-to-back semiconductor junctions with a breakdown voltage of the order of 3 to 3.5 V, essentially independent of the grain size. The macroscopic device is therefore a three-dimensional series–parallel network of a very large number of such microscopic junctions: the number of grains stacked in series across the electrodes fixes the overall *varistor voltage*, so that the breakdown voltage of the component can be set, almost at will, by choosing the thickness of the ceramic, while its current and energy capability are set by the electrode area. It is this granular, distributed structure — rather than a single planar junction as in a TVS diode — that gives the MOV its characteristic combination of high energy-absorption capability and strong non-linearity [40, 42]. Electrically, the device is commonly represented by the parallel combination of the intergranular capacitance C_p and a strongly voltage-dependent resistance R_p, placed in series with the nearly constant bulk resistance R_g of the ZnO grains; at low applied voltage R_p dominates and behaves almost ohmically, whereas at high current the grain resistance R_g becomes the limiting element [42].

The non-linear V–I characteristic. The defining property of the varistor is the extremely non-linear relationship between the voltage across it and the current through it, which over many decades of current is described with good accuracy by the empirical power law

$$I = k\,V^{\alpha}, \qquad \text{equivalently} \qquad V = \left(\frac{I}{k}\right)^{1/\alpha}, \tag{6.2}$$

where k is a constant fixed by the geometry and composition of the device and α is the *non-linearity coefficient*. For a good ZnO varistor α lies typically in the range 25–50, to be compared with $\alpha = 1$ for an ordinary ohmic resistor and $\alpha \approx 3$–7 for the older silicon-carbide varistors. Manufacturers more frequently quote the reciprocal exponent $\beta = 1/\alpha$, which is simply the slope of the characteristic on logarithmic axes and is written in the equivalent form $V = C\,I^{\beta}$, where C is the voltage at unit current; for ZnO β lies around 0.03–0.05, compared with $\beta \approx 0.4$ for a silicon-carbide varistor, $\beta = 1$ for an ohmic resistor and $\beta = 0$ for an ideal constant-voltage clamp [42]. The practical meaning of such a large exponent (equivalently, such a small β) is best appreciated

by noting that the voltage changes only as the $1/\alpha$ power of the current: with $\alpha = 30$ ($\beta \approx 0.033$), a change of the current by three orders of magnitude (a factor of 1000) produces a change of the voltage of only $1000^{1/30} \approx 1.26$, i.e. about 26 %. It is precisely this near-independence of the voltage from the current that allows the varistor to behave, to a first approximation, as the constant-voltage element assumed in the derivation of Equation (6.1).

The resulting characteristic is shown in Figure 6.5, plotted on logarithmic axes so that the power law of Equation (6.2) appears as a straight line whose slope equals $1/\alpha$. Three regions can be distinguished:

- **Leakage (pre-breakdown) region.** At voltages below the varistor voltage the intergranular barriers are not yet broken down and the device is highly resistive, conducting only a small, strongly temperature-dependent leakage current of the order of microamperes. This is the region in which the MOV of an SSCB sits during normal operation: the clamping voltage is deliberately chosen so that the recurring peak of the line voltage, $\hat{V}_s$, falls safely below the knee of the characteristic, so that the varistor draws negligible current and dissipates negligible power on every half-cycle.
- **Normal operating (clamping) region.** Above the varistor voltage the intergranular junctions break down and the device enters the strongly non-linear region described by Equation (6.2). The current rises by many orders of magnitude — from about 1 mA to several kiloamperes — while the voltage rises only modestly, producing the nearly flat plateau that constitutes the useful clamping action. This is the region in which the varistor operates during the energy-absorption phase (Phase 4 of Section 6.2), and the flat plateau is the direct cause of the flat-topped voltage spike observed in the breaker-voltage trace of Figure 6.1.
- **Upturn (high-current) region.** At very high currents the voltage drop across the bulk resistance of the conductive ZnO grains themselves can no longer be neglected, the characteristic loses its non-linearity and becomes approximately ohmic again, and the curve turns sharply upward. In this region the characteristic is well described by $V = C\,I^{\beta} + I\,R_s$, where the added term $I\,R_s$ represents the ohmic drop across the series grain resistance R_s (typically 0.05–0.5 Ω) [42]. This region sets the true maximum clamping voltage of the device and must be taken into account when the varistor is required to absorb the very large surge currents of a high-power interruption.

Datasheet parameters relevant to SSCB design. The parameters quoted by manufacturers map directly onto the design quantities of the energy-absorption branch [40, 42]:

- the *varistor voltage* V_N, conventionally specified as the voltage measured at a d.c. current of 1 mA, locates the knee of the characteristic;
- the *maximum continuous operating voltage* (MCOV), the highest a.c. (RMS) or d.c. voltage that may be applied indefinitely without appreciable heating. The a.c. rating is compared with the maximum RMS operating voltage and the d.c. rating

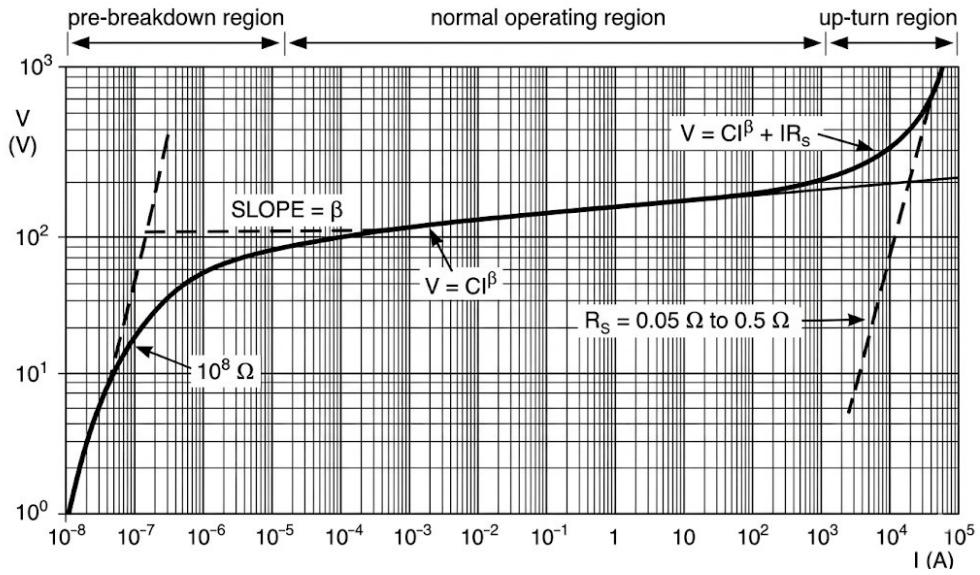


Figure 6.5. Typical V-I curve of a ZnO metal-oxide varistor.

with the maximum steady d.c. voltage, including tolerances. Separately, the clamping voltage must exceed the instantaneous supply voltage during interruption, as established in Section 6.2;

- the *clamping voltage* V_C, the voltage appearing across the device at a specified surge current and pulse shape (the standard $8/20\,\mu$s pulse is common), whose ratio to the varistor voltage, the *clamping ratio* $V_C/V_N \approx 1.5$–1.8, fixes the worst-case voltage stress imposed on the semiconductor switch;
- the *maximum peak surge current* and, most importantly for the breaker, the *maximum absorbed energy* (in joules, for a single pulse of stated duration), which must exceed with adequate margin the energy W_{MOV} of Equation (6.1) computed for the worst-case point-on-wave interruption.

Aging and thermal stability. A practical concern specific to the SSCB application is that, unlike a surge arrester that is called upon only rarely, the varistor of a circuit breaker is stressed close to its clamping region at *every* interruption. Repeated high-energy pulses gradually degrade the intergranular barriers: the leakage current in the pre-breakdown region slowly increases and the whole characteristic drifts downward, which in turn raises the standby power dissipation and, in the worst case, can lead to thermal runaway if the heat generated by the leakage current exceeds the rate at which it can be removed. For this reason the varistor is normally derated — both in energy and in operating voltage — relative to its nominal ratings, and the expected number of interruptions over the service life of the breaker becomes an explicit design parameter. This finite endurance of the energy-absorption branch is one of the practical limitations of present-day SSCBs [40, 42] and is discussed further among the open challenges of Chapter 9.

6.4.3 Gate driver circuits

The gate driver is the electronic interface between the low-power control system and the power semiconductor switch. In an SSCB, the gate driver must satisfy several stringent requirements [25, 38, 39]:

- Fast turn-off of the main switch, in order to minimize the time during which the device is subjected to the fault current. The turn-off transient is typically completed in less than 1 μs.
- Galvanic isolation between the control logic and the power circuit, usually implemented through optocouplers, fiber-optic links or isolated gate-drive transformers.
- Self-powered or fail-safe operation, so that the SSCB remains in a defined state even if the auxiliary power supply is lost during the fault.
- Protection features such as desaturation detection, Miller-clamp to prevent unintended turn-on during high $\mathrm{d}V/\mathrm{d}t$ transients, and active clamping, in which the drain-source overvoltage is fed back to the gate through a TVS stack.

For SSCBs employing series-connected devices, the gate driver must additionally ensure synchronous turn-off of all devices in the stack, in order to avoid uneven voltage sharing during the transient. Both single gate-drive (centralized) and multiple gate-drive (distributed) approaches have been proposed in the literature, each with its own trade-offs in terms of complexity, performance and reliability [43].

6.4.4 Fault detection and current sensing

The performance of an SSCB depends critically on the speed and accuracy with which it can detect a fault condition. Fault detection is based on the measurement of one or more electrical quantities and on the comparison of the measured values with predefined thresholds. The most common methods are:

- **Overcurrent detection.** The current through the SSCB is continuously measured and compared with a threshold, typically set at 2–3 times the rated current. As soon as the current exceeds the threshold, the trip command is issued. This is the simplest and most widely used method. Its response time depends on how far the threshold is set above the rated current – a slowly rising fault is detected late – and on the bandwidth of the current sensor.
- **Current slope detection ($\mathrm{d}i/\mathrm{d}t$).** Instead of (or in addition to) the absolute value of the current, the rate of change $\mathrm{d}i/\mathrm{d}t$ can be used as a trip criterion. Because the rate of change of the current is large from the very beginning of the fault, this method can provide a faster response than overcurrent detection alone, at the cost of an increased risk of false tripping due to load transients [39].
- **Desaturation detection.** In MOSFET- and IGBT-based SSCBs, an indirect indication of fault current is provided by the rise of the drain-source (or collector-emitter) voltage above the value corresponding to normal on-state operation. This method, originally developed for the protection of voltage-source inverters, can provide a

fast response, although a blanking time of the order of a microsecond is needed to ride out the turn-on transient. In an SSCB the main device operates permanently in the ohmic region, so what is implemented is strictly a drain-source voltage measurement against a threshold rather than desaturation detection in its original sense [2, 39].

Current sensors used in SSCBs include current shunts, Rogowski coils, Hall-effect sensors and giant-magnetoresistive (GMR) sensors. Shunts provide a very high bandwidth and good linearity but introduce additional conduction losses; Rogowski coils have a comparable bandwidth and no losses but cannot measure DC components; Hall-effect sensors are compact and inexpensive but have limited bandwidth. The choice depends on the specific requirements of the application [2, 10].

6.5 Applications of SSCBs

The combination of speed, controllability, longevity and arc-free operation makes SSCBs attractive across a broad spectrum of applications, each emphasizing a different subset of these benefits. The following list highlights the most representative deployment scenarios.

- **Industrial distribution and motor protection.** In industrial plants, fast and selective interruption protects sensitive equipment (variable-speed drives, robotics, controllers, UPS units) against downstream short circuits, limits voltage-sag propagation to the rest of the plant, and minimizes the let-through energy responsible for cable and transformer damage. The arc-free and maintenance-free character of the SSCB is especially valuable in continuous-process industries (chemical, oil-and-gas, steel, mining) where downtime is extremely costly and where the absence of an electric arc enables installation in classified hazardous areas.
- **Data centers and mission-critical loads.** Modern data centers and similar high-availability installations (hospitals, semiconductor fabs, telecom hubs, financial trading floors) require very high reliability and almost zero downtime. The submillisecond clearing time of SSCBs limits the propagation of voltage sags below the immunity threshold of sensitive equipment; the millions of operations supported without aging fit naturally with frequent reconfiguration; and the silent, vibration-free behavior is compatible with the strict environmental specifications of these facilities. Commercial low-voltage AC SSCBs are now available from several manufacturers specifically for data-center applications [11].
- **Residential and commercial distribution.** In low-voltage residential and commercial circuits, the SSCB can be combined with a residual-current device (RCD) to form a compact, arc-free and highly reliable protection unit. Adjustable current-time tripping characteristics, remote operation and self-diagnostics enable smart protection that adapts to the actual load profile, including increasing penetration of EV charging, heat pumps and rooftop PV.
- **Electric vehicle charging infrastructure.** Modern fast- and ultra-fast-charging

stations operate at high voltages and currents and demand fast disconnection in case of a fault, both to protect the vehicle and the charger and to enable plug-and-play functionality. SSCBs are increasingly used both on the AC input side of the charger and on the DC output side, where their arc-free operation is particularly valuable.

- **Renewable energy plants and inverter-based generation.** PV power stations, wind farms and battery energy storage systems contain large numbers of power-electronic converters with limited short-circuit withstand capability. Fast SSCBs allow individual converters and strings to be protected without affecting the operation of the rest of the plant, enable arc-free disconnection of DC strings, contribute to fault ride-through compliance, and support the bidirectional power flow typical of these installations [17, 19].
- **AC and DC microgrids.** In microgrids—and especially in islanded microgrids—the limited fault levels and the high penetration of converters demand fast and selective protection. SSCBs can be installed at the boundary between the microgrid and the main grid (enabling seamless transition between grid-connected and islanded operation) and at the level of individual feeders or loads (providing selective isolation of faults and supporting autonomous reconfiguration in response to disturbances).
- **Maritime and aerospace power systems.** In hybrid- and all-electric ships and in more-electric aircraft, weight, volume, reliability and the absence of arcing are at a premium. The compactness, fast operation, silent behavior and very long lifetime of SSCBs make them especially attractive in these environments, where mechanical wear and corrosive atmospheres rapidly degrade conventional switchgear. Wide-bandgap devices further benefit these applications thanks to their tolerance of elevated ambient temperatures.
- **Railway and traction power supply.** Railway substations and on-board converters benefit from fast SSCBs for the protection of catenary feeders, regenerative-braking converters and auxiliary services. The very high number of switching cycles encountered in traction service makes the long lifetime of SSCBs particularly attractive.
- **Defense and special applications.** Pulsed-power systems, radar installations and mobile generation units require switchgear capable of operating reliably under extreme conditions and of responding to events much faster than mechanical breakers permit. SSCBs are well suited to these niche but technologically demanding applications.

Across this entire spectrum, the same underlying properties—ultra-fast interruption, arc-free operation, controllability, longevity and integration with digital protection—translate into concrete benefits: better protection of sensitive equipment, reduced downtime, lower maintenance, smaller and lighter installations, improved system stability and a smaller environmental footprint. Their relative importance varies from one application to another, but the technology is in all cases a single, coherent answer to

the requirements of modern AC power systems.

6.5.1 Fault-level limitation and renewable-energy hosting capacity

A benefit that cuts across several of the applications listed above, and that is of particular relevance to networks with a high share of renewable energy, deserves separate mention: the ability of a solid-state breaker to limit the contribution that a source makes to the short-circuit current of the network.

Every busbar and every piece of switchgear in a distribution network is rated for a maximum short-circuit current that it can withstand and, in the case of a breaker, interrupt. As more distributed generation is connected to a feeder, each additional source contributes to the total fault current, so that the prospective short-circuit level at the network nodes rises. Once this level approaches the withstand or breaking rating of the existing equipment, the hosting capacity of the network for further generation is effectively exhausted, and any additional connection requires the costly replacement or upgrade of switchgear, busbars and transformers. The fault level—rather than the thermal or voltage limits of the lines—then becomes the binding constraint on renewable-energy integration.

A solid-state breaker alleviates this constraint by exploiting the time structure of the short-circuit current. The fault current does not reach its full magnitude instantaneously: it builds up from the instant of the fault, passing through a large subtransient peak before settling. A conventional electromechanical breaker, with a clearing time of the order of tens of milliseconds, allows this current to develop fully, so that the equipment must withstand the entire peak and the associated let-through I^2t. A solid-state breaker, by contrast, interrupts within a fraction of a millisecond—before the current can reach its peak—and, when operated in the current-limiting mode described in Chapter 7, actively bounds the current for a prescribed interval within the thermal and energy limits of the breaker. The peak current and let-through I^2t from the protected source can therefore be reduced.

This potential benefit requires verification of equipment withstand, selective coordination and the applicable fault-ride-through requirements; rapid disconnection of a healthy generating unit during an external fault cannot be assumed permissible [3]. The benefit concerns the actual limited current and its duration, rather than an automatic change in the prospective short-circuit level of the unprotected network.

With these conditions satisfied, fault-current limitation may permit additional distributed generation where equipment short-circuit withstand is the binding constraint, potentially avoiding some equipment upgrades [44]. This is a network-specific planning outcome, not an automatic consequence of installing a fast breaker. Thermal loading and steady-state voltage limits remain separate constraints. This network-level benefit is revisited in Chapter 7, where the fast interruption of the fault contribution of a local synchronous generator is demonstrated in a three-phase distribution feeder.

Chapter 7

Modeling and Simulation Results

The preceding chapters established the operating principle, the device-level characteristics and the system-level architecture of solid-state circuit breakers. This chapter complements that theoretical treatment with a set of time-domain simulations carried out in MATLAB/Simulink, using the Simscape Electrical library. The objective is twofold: first, to verify that the SSCB and its control logic behave as predicted by the theory; and second, to quantify the advantage of the solid-state breaker over more conventional interruption technologies under identical fault conditions.

The simulation work is organized in two parts. The present chapter first considers a single-phase system, which serves as the fundamental test case in which the operation of the breaker and of its control system is validated in detail (Section 7.1). The single-phase principle is then extended to a three-phase network, both for a grid-feeding configuration with passive loads and for a configuration that additionally includes a local generator (Section 7.2).

7.1 Single-phase system

7.1.1 Test circuit and simulation parameters

The single-phase test circuit consists of a sinusoidal voltage source feeding a series resistive–inductive load through the solid-state circuit breaker. The source represents a 230 V (RMS), 50 Hz low-voltage network, with a small series resistance and inductance accounting for the line impedance. A fault is introduced in parallel with the load by means of a controllable fault branch, whose resistance drops from a very high (open-circuit) value to a small short-circuit value at the instant $t = 0.1\,\mathrm{s}$. The breaker is placed in series between the source and the load, so that it carries the full line current and is able to isolate the fault from the source.

The complete set of parameters used in the single-phase simulations is summarized in Table 7.1. The load resistance and inductance are chosen so that the steady-state peak line current is of the order of 58 A, which is well below the 100 A detection threshold of the breaker and therefore represents normal operating conditions.

7.1.2 Power stage and energy-absorption branch

The power stage of the breaker, shown in Figure 7.1, is implemented as a back-to-back pair of silicon-carbide power MOSFETs, in accordance with the bidirectional topology discussed in Section 6.3. The two devices are modeled using the manufacturer-provided thermal model of the STMicroelectronics SCTWA90N65G2V, so that the conduction losses, the switching losses and the resulting junction temperature are computed self-consistently during the simulation. The common-source arrangement of the two tran-

Table 7.1. Parameters of the single-phase simulation model.

Subsystem	Parameter	Value
Source	Voltage (RMS / peak)	230 V / $230\sqrt{2} \approx 325$ V
	Frequency	50 Hz
Line	Resistance	0.01 Ω
	Inductance	0.5 mH
Load	Resistance	4.6 Ω
	Inductance	10 mH
Main switch	Device	SiC MOSFET, ST SCTWA90N65G2V (back-to-back pair)
	On-state resistance $R_{ds(on)}$	0.017 Ω
	Switching energy E_{on} / E_{off}	22.86 mJ / 17.14 mJ
Clamping	MOV clamping voltage	480 V
Thermal	Ambient temperature	25 °C
	Junction-to-ambient resistance	2 K/W
	Initial junction temperature	80 °C

sistors allows the breaker to block voltage and to conduct current in either polarity, as required for an AC breaker.

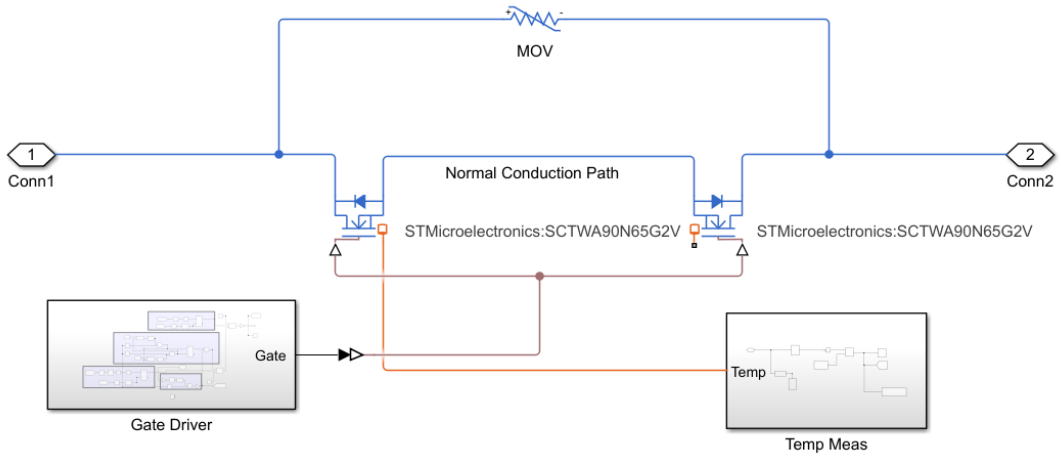


Figure 7.1. Power stage of the single-phase SSCB: back-to-back SiC MOSFET pair, parallel metal-oxide varistor for voltage clamping, gate-driver subsystem and thermal-measurement subsystem.

A metal-oxide varistor is connected in parallel with the switch to absorb the inductive energy of the network at the instant of interruption and to clamp the voltage across the devices to a safe value, following the principle described in Section 6.2. Its clamping voltage is set to 480 V; for a 230 V system this corresponds to approximately 1.5 times the peak source voltage, which keeps the voltage stress on the MOSFETs comfortably below their rated blocking voltage while still allowing a rapid decay of the interrupted

current, as discussed in Section 6.2.

7.1.3 Control architecture

The control logic that generates the gate signal of the breaker is shown in Figure 7.2. It is organized into three functional blocks, which operate on the measured line current and on the measured switch temperature and which together determine the state of the gate command.

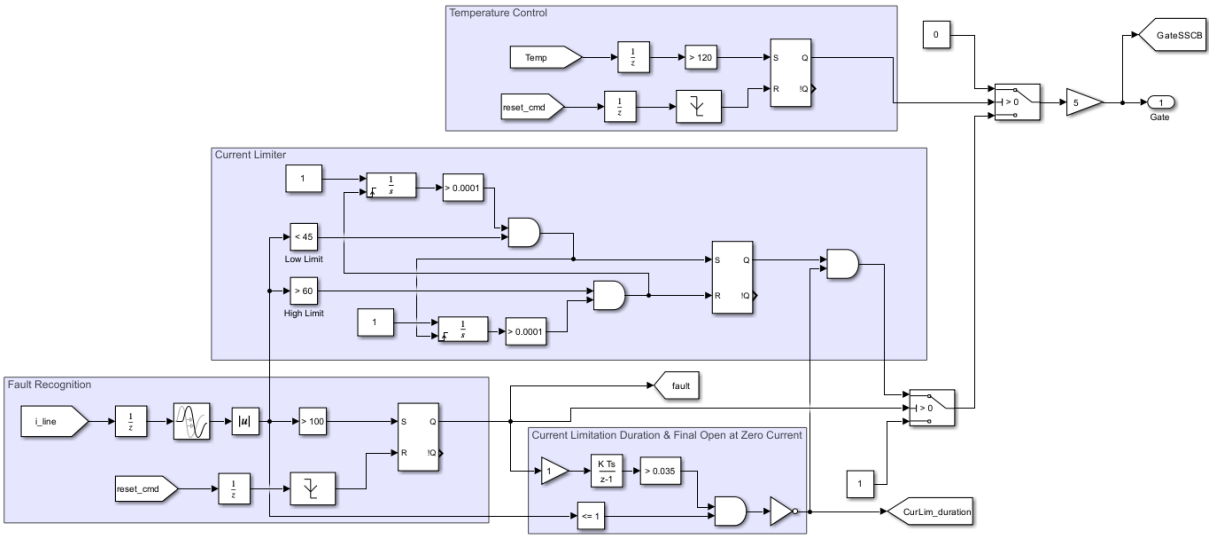


Figure 7.2. Control logic of the single-phase SSCB, comprising the fault-recognition block, the current-limiter block and the temperature-control block.

- **Fault recognition.** The absolute value of the measured line current is compared with a fixed threshold of 100 A, which plays the role of the current-sensor trip level I_{sens}. When the current exceeds this threshold, a set–reset latch is set and a fault is declared. The latch retains the fault state until it is explicitly cleared by an external reset command, so that the breaker does not re-close spontaneously while the fault is still present. This corresponds to the overcurrent-detection method described in Section 6.2.
- **Current limiter.** Once a fault has been detected, the breaker does not necessarily interrupt the current immediately; instead, it can be operated in a current-limiting mode, in which the gate signal is switched on and off so as to keep the line current within a predefined hysteresis band. The upper and lower limits of this band are determined by the circuit characteristics in the same way as in any classical hysteretic current controller: for a given line inductance L and applied voltage v, the rate of change of the current during the on- and off-intervals is $\mathrm{d}i/\mathrm{d}t = v/L$, and it is this ramp rate—together with the width of the band—that sets the natural switching frequency of the hysteretic loop. The mechanism is illustrated schematically in Figure 7.3.

  In a standard hysteretic controller this frequency would be determined solely by the circuit, and could in principle become arbitrarily high if the band is narrow

or the inductance is small. For a power semiconductor, however, each commutation incurs a fixed switching energy loss, so an unbounded switching frequency translates directly into unbounded switching losses and, ultimately, into thermal destruction of the device. The control strategy adopted here addresses this by imposing a *minimum dwell time* $t_{\min}$ in each switching state, implemented by two integrators with a comparison threshold in the control logic. This minimum dwell time is the design parameter that the engineer sets directly; it translates into a well-defined upper bound on the switching frequency:

$$f_{sw,\max} = \frac{1}{2\,t_{\min}}.$$

In the present simulation $t_{\min} = 0.2\,\mathrm{ms}$, giving $f_{sw,\max} = 2.5\,\mathrm{kHz}$. What the designer therefore controls is not the band width directly, but the *worst-case switching frequency*: by choosing $t_{\min}$ the maximum number of commutations per second—and hence the maximum switching loss contribution—is capped independently of the circuit parameters, providing an explicit and predictable means of protecting the semiconductor from excessive switching stress. The band width, on the other hand, is a consequence of this choice together with the network inductance and the instantaneous voltage, and determines the quality of the current tracking as discussed in Section 7.1.6.

The total duration of the current-limiting phase is set by a separate timer (the discrete integrator at the output of the block); in the results presented below this duration is set to 0.035 s, after which the breaker performs a definitive interruption at the first natural *current zero*. Opening at a current zero means that the magnetic energy trapped in the line, $\frac{1}{2}Li^2$, is essentially zero at the instant of interruption, so that almost no energy is forced into the varistor and the MOSFETs commutate under zero-current conditions. This protects both the power semiconductors and the metal-oxide varistor from the large turn-off transient that a hard interruption at an arbitrary point of the cycle would otherwise produce.

- **Temperature control.** The junction temperature of the switch is monitored and compared with a thermal limit of 120 °C. If this limit is exceeded, a second set–reset latch is set and the gate command is forced off, irrespective of the state of the other two blocks, thus providing an independent over-temperature protection. As with the fault-recognition latch, the thermal latch is cleared only by an external reset command.

The outputs of the three blocks are combined so that the gate command is asserted only when no fault, no current-limiting chopping command and no over-temperature condition require the switch to be off. The resulting logic signal is scaled to the gate-drive voltage level and applied to the gate driver of the power stage through a fixed propagation delay of 20 μs, which represents the finite reaction time of the sensing and gate-drive chain.

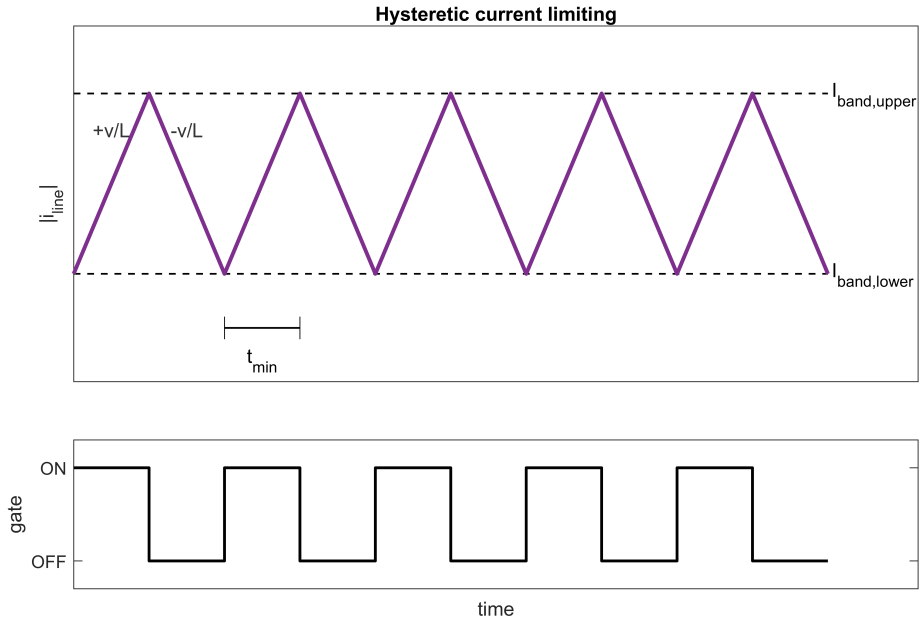


Figure 7.3. Principle of the hysteretic current limiter. While the switch is on, the line current ramps up with slope $+v/L$; when it reaches the upper edge of the band the gate is removed and the current ramps down with slope $-v/L$ until the lower edge is reached, at which point the switch is turned on again. The minimum dwell time $t_{\min}$ enforced in each state caps the switching frequency at $f_{sw,\max} = 1/(2t_{\min})$, while the resulting band width follows from $t_{\min}$ together with the ramp rate v/L.

7.1.4 Case 1: direct interruption

In the first scenario the current-limiting function is disabled, so that the breaker performs a direct interruption as soon as the fault is detected. The resulting line current, load voltage and switch temperature are shown in Figure 7.4.

During normal operation, up to $t = 0.1\,\mathrm{s}$, the line current is a sinusoid of approximately 58 A peak and the load voltage follows the source voltage. When the fault is applied at $t = 0.1\,\mathrm{s}$, the current begins to rise rapidly; as soon as it reaches the 100 A threshold, the fault-recognition block trips the breaker and the current is forced to zero in less than a millisecond. The load voltage collapses to zero at the same instant, confirming that the fault has been isolated from the source. After interruption the switch no longer dissipates power, and its junction temperature decays exponentially from its initial value towards the ambient temperature, with a time constant set by the junction-to-ambient thermal resistance of the thermal model. This scenario demonstrates the fundamental advantage of the solid-state breaker: the fault current is interrupted almost instantaneously, before it can reach a destructive magnitude.

7.1.5 Case 2: interruption with current limiting

In the second scenario the current-limiting function is enabled. After the fault is detected, the breaker enters the current-limiting mode described in Section 7.1.3, in which the gate signal is chopped at a maximum frequency of 2.5 kHz so as to keep the line current

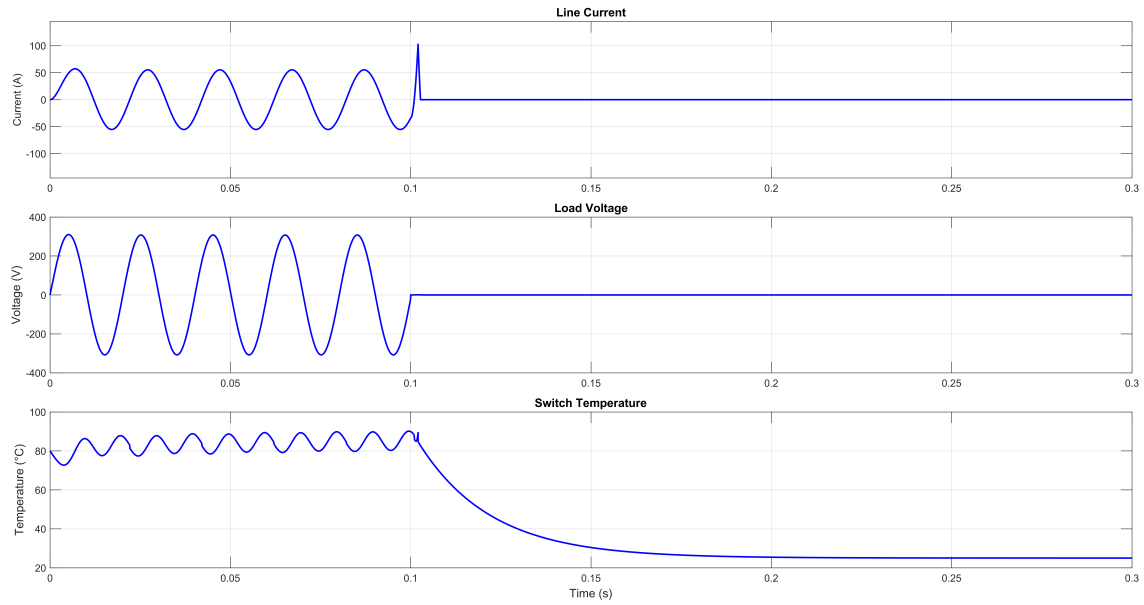


Figure 7.4. Single-phase SSCB performing a direct interruption: line current (top), load voltage (middle) and switch junction temperature (bottom). The fault is applied at $t = 0.1\,\mathrm{s}$.

within a narrow band centered on the desired RMS level, before performing a definitive interruption at the end of the limiting window. The corresponding waveforms are shown in Figure 7.5.

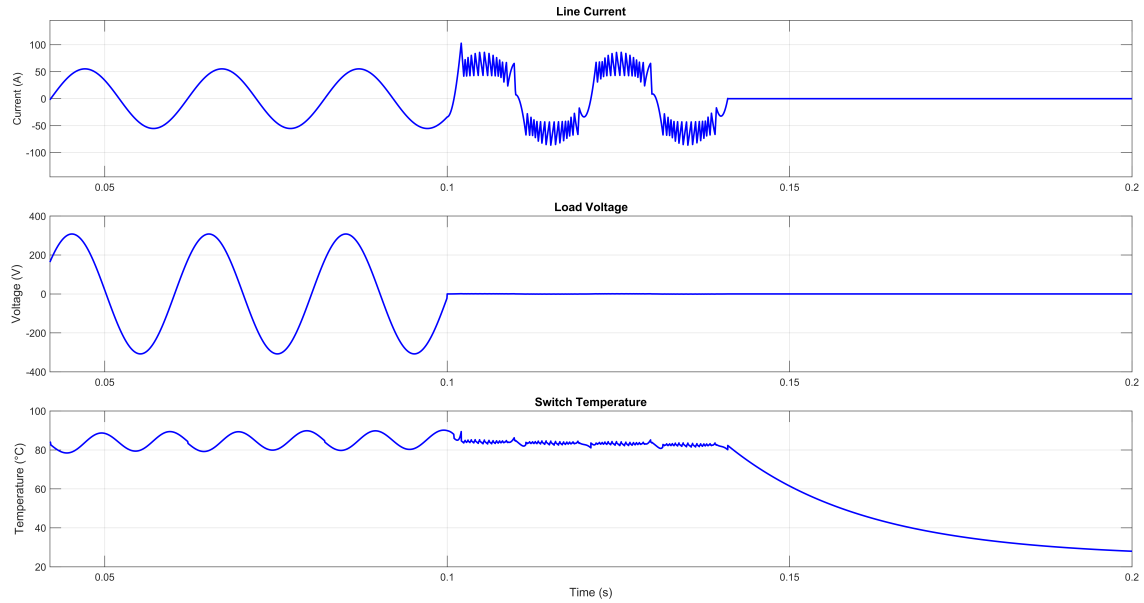


Figure 7.5. Single-phase SSCB operating in current-limiting mode at a maximum switching frequency of 2.5 kHz*: line current (top), load voltage (middle) and switch junction temperature (bottom).*

The line current is held within the limiting band for the duration of the limiting window (0.04 s), as opposed to being interrupted immediately. The high-frequency chopping of the current is clearly visible in the top trace. The benefit of this mode is that the fault current is kept under control without a sudden interruption, which reduces the voltage transients imposed on the network and gives any upstream or downstream

protection devices the opportunity to coordinate. The cost is that the switch continues to conduct—and therefore to dissipate power—during the limiting phase, which is reflected in the switch temperature: instead of decaying immediately as in Case 1, the temperature remains elevated for the duration of the limiting window and only decays once the current has been definitively interrupted. This trade-off between let-through current and thermal stress is one of the central design considerations for current-limiting SSCBs.

7.1.6 Effect of the limiting switching frequency

The maximum switching frequency of the current limiter is a free design parameter, set by the minimum dwell time enforced by the integrators in the control logic (Section 7.1.3). To investigate its influence, the current-limiting scenario of Section 7.1.5 was repeated for three values of the maximum switching frequency—1 kHz, 2.5 kHz and 5 kHz—corresponding to minimum dwell times of 0.5 ms, 0.2 ms and 0.1 ms respectively. The 2.5 kHz case is the one already presented in Figure 7.5; the 1 kHz and 5 kHz cases are shown in Figures 7.6 and 7.7.

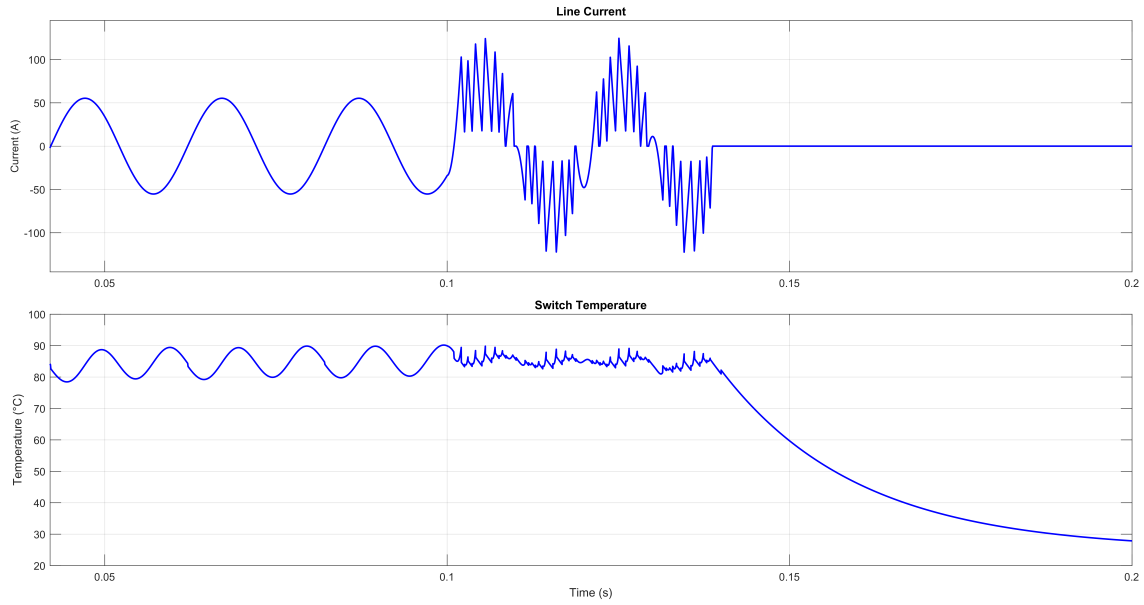


Figure 7.6. Current limiting at a maximum switching frequency of 1 kHz*: line current (top) and switch junction temperature (bottom).*

The switching frequency primarily controls how faithfully the hysteretic limiter is able to confine the line current to the prescribed band. Because the fault current is driven through the line inductance, its rate of change $\mathrm{d}i/\mathrm{d}t = v/L$ is finite; during each switching interval the current therefore continues to ramp until the next switching action takes place. The longer the dwell time—that is, the lower the switching frequency—the further the current is allowed to deviate from the band before it is corrected. This is clearly visible in the results: at 1 kHz (Figure 7.6) the long dwell time allows the current to swing well beyond the band, reaching peaks of the order of 130 A, whereas at 5 kHz (Figure 7.7) the current is confined closely to the band, with peaks at 65 A, so that it

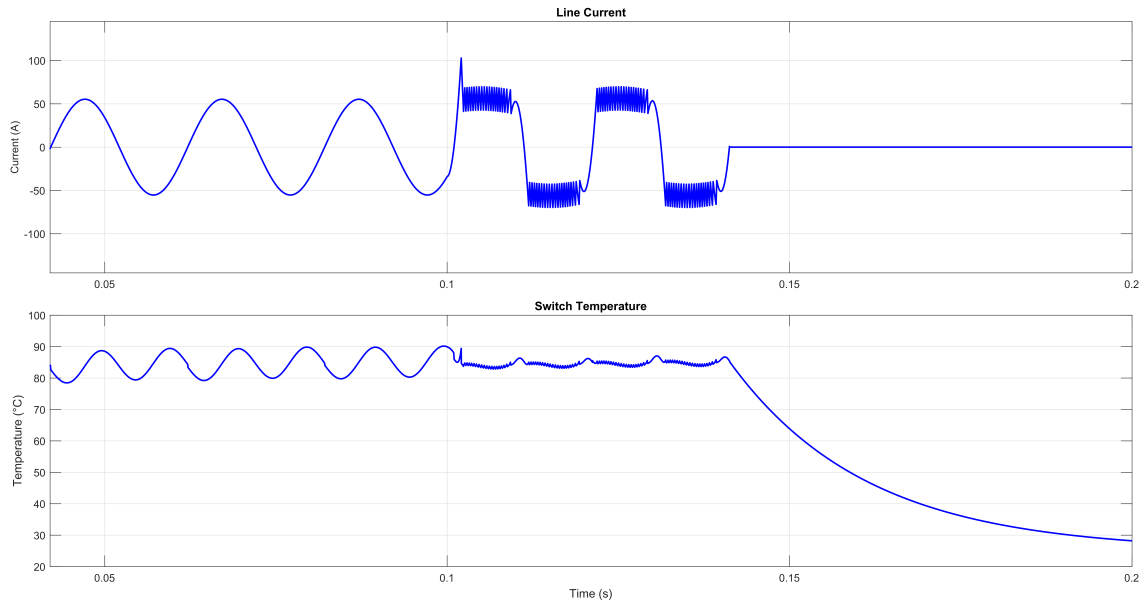


Figure 7.7. Current limiting at a maximum switching frequency of 5 kHz*: line current (top) and switch junction temperature (bottom).*

tracks the underlying sinusoid much more cleanly. The 2.5 kHz case lies between these two extremes.

The junction temperature of the switch exhibits a qualitatively different behavior from Case 1, but one that deserves careful interpretation. Rather than decaying immediately after the fault is detected, the temperature remains approximately at its pre-fault steady-state value for the entire duration of the limiting window, and only begins to fall once the definitive interruption has been performed.

This behavior is, in fact, the expected and intended outcome of the current-limiting strategy. The hysteretic controller is designed to hold the line current close to the RMS value that would flow under normal operating conditions; it follows that the average power dissipated in the switch during the limiting phase is comparable to the dissipation in normal operation. The junction temperature, which responds to this average power filtered through the thermal inertia of the device, therefore *stays at roughly the same level it would have reached anyway*—it neither rises sharply as it would under a sustained overcurrent, nor falls as it would if the switch were opened. In this sense the current limiter is thermally transparent: it keeps the device within its normal operating envelope while actively bounding the fault current delivered to the network. Table 7.2 summarizes how the maximum limiting switching frequency affects the let-through current and the resulting switch temperature.

The practical conclusion is that, over the range and for the device model examined here, the choice of switching frequency is governed essentially by the quality of the current tracking and the resulting let-through ripple, rather than by a thermal constraint: a higher switching frequency yields a cleaner, more sinusoidal limited current at the cost of more frequent commutations, while the junction temperature stays within a safe and almost constant range in all cases. It should nevertheless be emphasized that this near-insensitivity is specific to the device loss model and to the network parameters

Table 7.2. Effect of the maximum limiting switching frequency on the let-through current and on the switch temperature. The current and temperature values are approximate, read from the simulation waveforms during the limiting window.

Max. switching frequency	**Min. dwell time**	**Peak $\lvert i_{line}\rvert$ (limiting phase)**	**T_j during limiting phase**
1 kHz	0.5 ms	$\approx$ 130 A	$\approx$ 85–90 °C
2.5 kHz	0.2 ms	$\approx$ 90 A	$\approx$ 80–85 °C
5 kHz	0.1 ms	$\approx$ 65 A	$\approx$ 82–85 °C

used; a different ratio of switching to conduction losses, a different line inductance or a wider band could make the thermal behavior more sensitive to the switching frequency.

Note on the thermal model. The junction-temperature traces need to be read with care, and this is the first point at which the thermal behavior of the device has been discussed. The thermal sub-model is used in this work to demonstrate the operation of the thermal-protection function and to illustrate the qualitative thermal behavior of the breaker during and after a fault. It is not intended as a calibrated electro-thermal prediction of the specific device: the junction temperature of a single representative transistor is monitored, and the thermal inertia of that device has been deliberately reduced so that the response of the temperature-control loop can be clearly observed within the simulated time window. A more detailed electro-thermal model, accounting for both devices of the back-to-back pair and for the realistic thermal masses, is identified as a possible direction for future work in Chapter 9.

7.1.7 Energy management of the clamping varistor during current limiting

The current-limiting strategy analyzed so far was described purely from the point of view of the line current and the switch, without reference to the clamping element. In that idealized picture the hysteretic chopping confines the fault current to the prescribed band and, as shown in Section 7.1.6, is essentially thermally transparent to the semiconductor. A practical implementation, however, cannot ignore the metal-oxide varistor (MOV) connected across the switch: a strategy that is benign for the MOSFETs may be destructive for the varistor. This subsection therefore re-examines the same current-limiting scenario with the energy stress on the MOV as the figure of merit, and introduces the circuit modification required to make the chopping operation sustainable.

Why repetitive chopping is incompatible with a single-shot MOV. In a direct interruption (Case 1) the MOV absorbs a single pulse of inductive energy $\frac{1}{2}Li^2$ when the switch opens under fault current; this single event is the most demanding one and sets the dimensioning criterion for the varistor. In current-limiting mode, by contrast, the switch is opened and reclosed many times within the limiting window, and if the MOV

were left to clamp every one of these turn-off transitions it would be forced to absorb a comparable energy pulse at each commutation. As the comparison below shows, the cumulative energy then grows as a staircase that exceeds the single-shot rating of the device by more than an order of magnitude. The chopping operation is therefore not viable unless the inductive energy is diverted away from the varistor at each turn-off; this is the role of the controlled freewheeling discharge path introduced next.

The controlled freewheeling discharge path. The discharge path—shown in Figure 7.8—diverts the bulk of the commutated inductive energy away from the varistor at each turn-off. The path consists of a diode bridge placed around the back-to-back MOSFET pair, rectifying the AC line current onto a DC bus, across which a controlled switch and dump resistor R_{dump} are connected in series. When the main switch opens during a chopping cycle, the line current commutates into this path and decays through R_{dump} with time constant $\tau = L/R_{\text{dump}}$, rather than flowing through the MOV. The discharge switch is enabled only during current-limiting mode; in direct-interruption mode it remains open, leaving the MOV to perform its conventional single-shot clamping function unaffected.

The rectifying bridge is what makes this arrangement attractive in a single-phase AC application, and the choice deserves a brief justification. Functionally the branch behaves as a *crowbar*: a controlled element is fired to provide a low-impedance bypass into which the inductive current is dumped, and it conducts until that current decays. A crowbar connected directly to the AC side, however, would have to conduct the fault current in both polarities, which requires a *bidirectional* controlled device—two anti-series thyristors (or MOSFETs), or a triac. This doubles the number of controlled power devices and, more importantly, forces at least one gate drive to be referenced to a floating node, with its own isolated supply. By rectifying the line current first, the dump branch instead sits on a DC bus of fixed polarity and can be controlled by a *single* device whose reference terminal is tied to the negative rail, so that an ordinary non-isolated gate drive suffices. The four bridge diodes are passive, inexpensive and rugged against surge, and add negligible cost and complexity compared with a second controlled channel and its isolated drive. This is why rectification, rather than a directly-connected bidirectional crowbar, was adopted for the discharge path.

The MOV therefore acts as a *backup voltage clamp* during chopping rather than as a repetitive energy absorber. Its clamping threshold is reached at certain instants—particularly at the beginning of the limiting window, when the line current is at its highest within the chopping band—but the varistor current i_{MOV} at those instants is small, since the freewheeling branch carries the bulk of the commutated energy. Because the absorbed energy is governed by the product $V_{\text{MOV}} \cdot i_{\text{MOV}}$, the cumulative varistor stress over the entire limiting window remains low despite the large number of switching cycles.

Quantitative comparison. The comparison was carried out for the 2.5 kHz current-limiting case (minimum dwell time $t_{\min} = 0.2\,\text{ms}$ per switching action) of Section 7.1.6. Figures 7.9 and 7.10 show the switch current, switch voltage and MOV current without

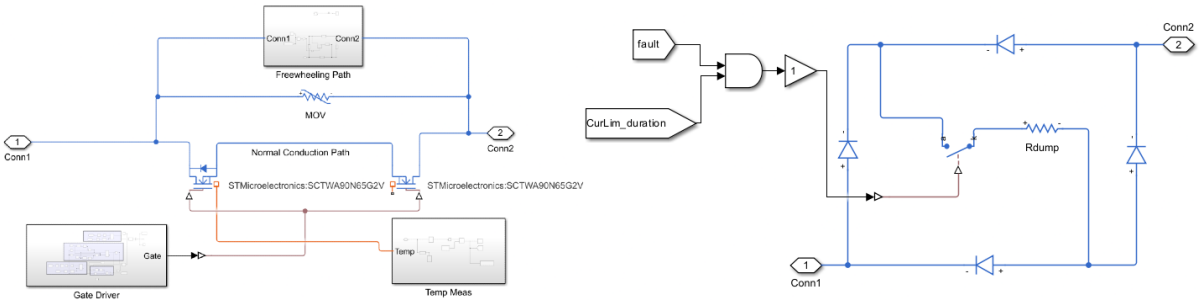


Figure 7.8. Topology of the controlled freewheeling discharge path: a diode bridge rectifies the AC line current to a DC bus across which a controlled switch and R_{dump} provide a controlled decay path for the inductive energy at each turn-off, relieving the MOV of repetitive switching stress.

and with the freewheeling path respectively. Without the path (Figure 7.9), a varistor-current pulse is drawn at almost every turn-off, so that i_{MOV} tracks the chopping envelope throughout the limiting window; with the path active (Figure 7.10), the MOV conducts only a single significant pulse at the very first turn-off and remains essentially inactive thereafter, while the switch voltage is still clamped at every transition.

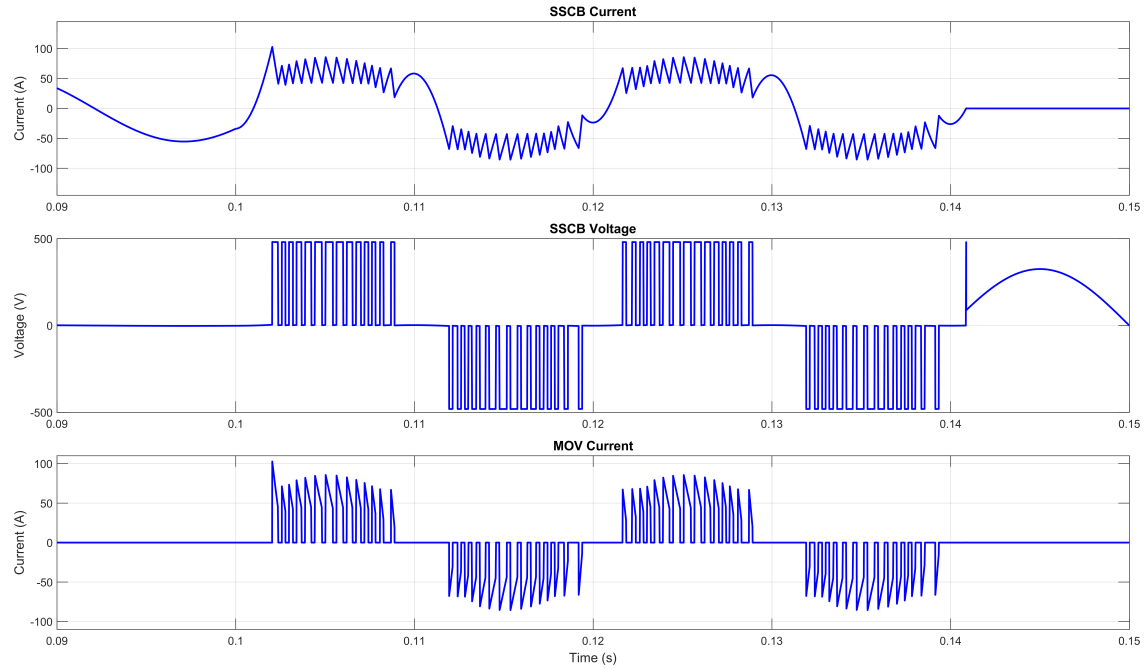


Figure 7.9. Current limiting at $f_{\mathrm{max}} = 2.5\,\mathrm{kHz}$ without the freewheeling path: switch current (top), switch voltage (middle) and MOV current (bottom). The varistor draws a current pulse at nearly every turn-off across the whole limiting window.

Figure 7.11 quantifies the effect. Without the freewheeling path, the MOV energy accumulates as a staircase over the 40 ms limiting window, reaching approximately 450 J—more than thirty times the 14 J absorbed in a direct interruption. With the freewheeling path active, the cumulative varistor energy is reduced to approximately 12 J, roughly a factor of forty below the no-freewheeling case and comparable to the energy of a single direct interruption. This confirms the operating principle described above: the freewheeling branch carries the bulk of the commutated current at each

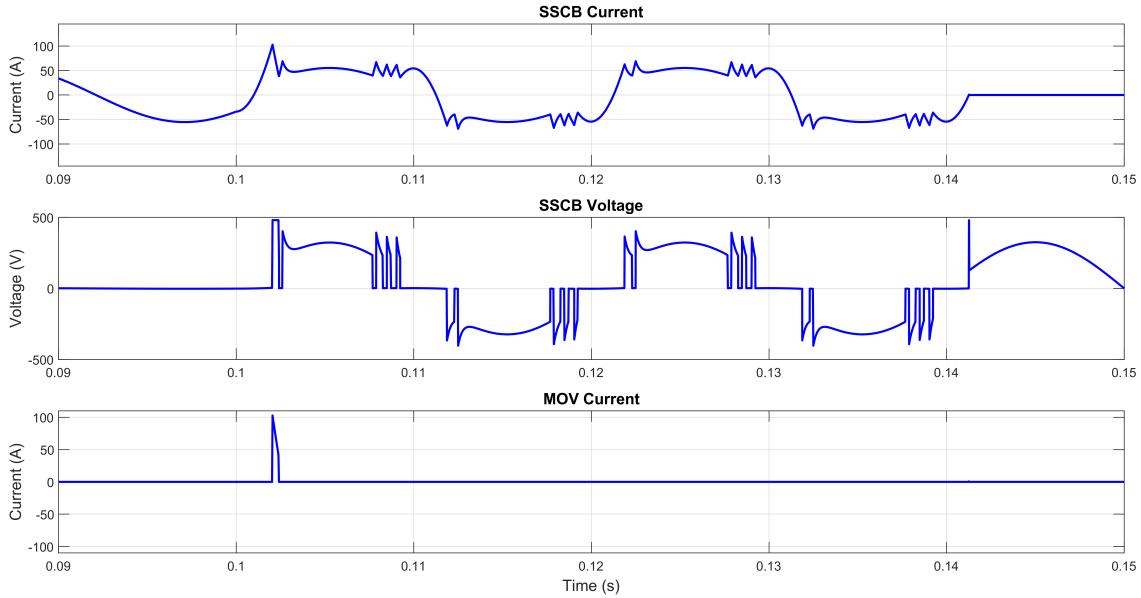


Figure 7.10. Current limiting at $f_{\max} = 2.5\,\text{kHz}$ *with the controlled freewheeling path: switch current (top), switch voltage (middle) and MOV current (bottom). The varistor conducts only at the first turn-off and is essentially inactive thereafter, while the switch voltage is still clamped at every transition.*

turn-off, so that the varistor conducts only a negligible residual fraction and its energy absorption is effectively confined to the first fault transient.

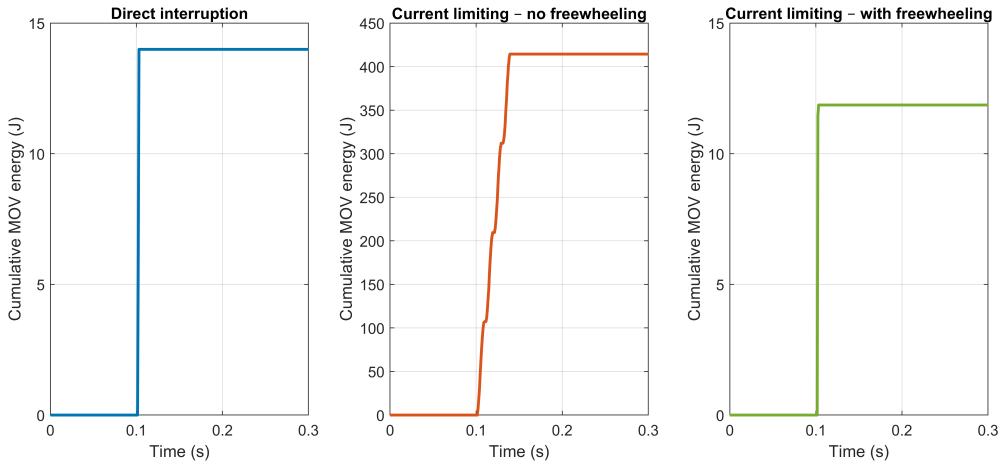


Figure 7.11. Cumulative energy $\int V_{\text{MOV}}\, i_{\text{MOV}}\, \mathrm{d}t$ *absorbed by the MOV in the three operating scenarios: direct interruption, current limiting without freewheeling path, and current limiting with freewheeling path.*

Alternative varistor protection strategies. For completeness, alternative circuit-level approaches to managing the varistor energy during repetitive switching are noted here, even though they are not implemented in the present simulation. An *active clamp* replaces the passive R_{dump} with a controlled semiconductor switch, allowing the discharge current to be regulated precisely and, in principle, a fraction of the inductive energy to be recovered to a local storage element. An *RC or RCD turn-off snubber* placed

directly across the switch reduces the peak $\mathrm{d}v/\mathrm{d}t$ at turn-off, limiting the instantaneous voltage stress on the MOV and spreading its energy absorption over a longer interval. Finally, an *LC resonant commutation branch* can be designed to drive the switch current to zero before the gate signal is removed, so that each interruption—whether partial or final—occurs under near-zero-current conditions and releases essentially no inductive energy into the clamping circuit; this is the operating principle of the hybrid resonant breaker topologies reviewed in Chapter 4. Each strategy represents a different point on the design space defined by circuit complexity, energy recovery capability, switching speed and varistor dimensioning, and the choice among them is ultimately governed by the specific device ratings and duty-cycle requirements of the application.

A further alternative is to replace the standard single-pulse MOV with a *multi-pulse* varistor specifically engineered to withstand a large number of successive energy injections. Standard varistors are characterized by a single non-repetitive peak current rating; multi-pulse devices, by contrast, specify a repetitive-pulse energy envelope as a function of pulse count and inter-pulse cooling interval, achieved through a larger active cross-section and an improved zinc-oxide microstructure [40]. In principle, such a device could absorb the repetitive chopping transients directly, without a separate freewheeling branch, at the cost of a larger and more expensive component compared to the additional circuit complexity of the controlled discharge path.

7.1.8 Comparison with resonant and electromechanical breakers

To place the performance of the SSCB in context, the same fault was applied to the same network when protected by three different interruption technologies: the solid-state breaker studied in this work; a circuit breaker employing an LC resonant commutation circuit; and an electromechanical circuit breaker (EMCB). A reference case without any breaker is also included. The resulting line currents are compared in Figure 7.12.

The four cases differ by orders of magnitude. With no breaker present, the fault current develops into a large, slowly-decaying oscillation: it follows the natural short-circuit response of the network, with a first peak of approximately 1260 A and subsequent peaks of roughly 1130, 1020, 950 and 890 A as the DC offset decays, and it is never interrupted. The electromechanical breaker follows *exactly the same trajectory* as the no-breaker case—because until its contacts part it is simply a closed switch—and is distinguished from it only by the fact that the current is finally forced to zero at a natural current zero around $t = 0.137\,\mathrm{s}$, after two full half-cycles of fault current have already flowed. The peak let-through current of the EMCB is therefore the same ≈ 1260 A first peak as the uninterrupted case; its mechanical opening delay (of the order of 30 ms) buys nothing in terms of peak current and merely terminates the oscillation a few cycles in. The breaker with the LC resonant circuit performs markedly better: it drives the device current to zero through forced commutation, so that the current is interrupted after reaching approximately 660 A, roughly half the EMCB peak. The solid-state breaker interrupts the current almost as soon as it crosses the 100 A detection threshold, holding the let-through current to a value only marginally above the threshold and clearing the fault within a fraction of a millisecond.

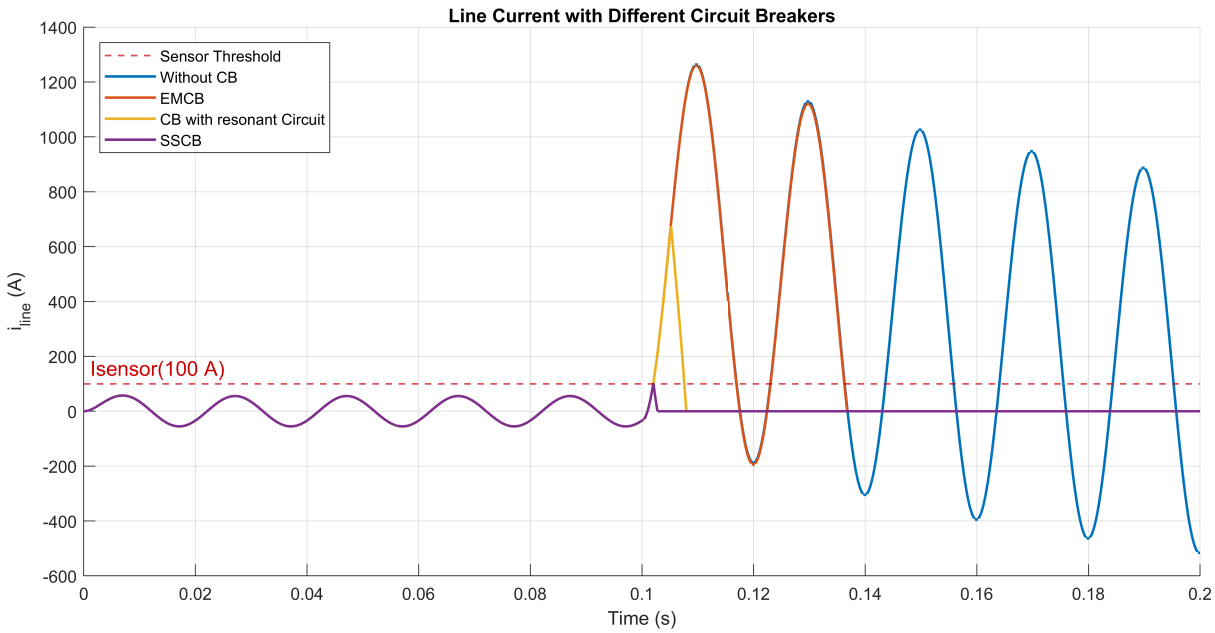


Figure 7.12. Line current during the fault for different interruption technologies: without breaker, solid-state breaker (SSCB), circuit breaker with LC resonant circuit, and electromechanical breaker (EMCB). The dashed line marks the 100 A *detection threshold.*

These observations are summarized in Table 7.3, which lists, for each case, the approximate interruption instant and the peak let-through current read from Figure 7.12.

Table 7.3. Interruption time and peak let-through current for the four cases of Figure 7.12. The fault is applied at $t = 0.1$ s*; values are read from the simulated waveforms.*

Interruption technology	**Interruption instant**	**Peak let-through current**
Without breaker	not interrupted	1260 A (first peak)
Electromechanical (EMCB)	36 ms	1260 A
LC resonant breaker	5 ms	680 A
Solid-state (SSCB)	0.8 ms	100 A

The peak current, however, tells only part of the story. What ultimately stresses the protected equipment is not the peak alone but the *let-through energy*—the integral of the current (squared) over the time for which it is allowed to flow—since this is what determines the thermal and mechanical loading of conductors, joints and downstream devices. Because the EMCB allows the full fault current to flow for two half-cycles while the SSCB interrupts within a fraction of a millisecond, the difference in let-through energy is far larger than the difference in peak current alone would suggest. Figure 7.13 makes this explicit by plotting the cumulative let-through energy $\int i^2\,\mathrm{d}t$ (a quantity proportional to the thermal stress, and equal to the I^2t rating against which conductors and semiconductors are dimensioned) for each of the four cases.

This comparison quantifies, for the specific network considered, the principal qualitative advantage of solid-state breakers that was anticipated in the review of Chapter 4: their interruption time is several orders of magnitude shorter than that of electromechan-

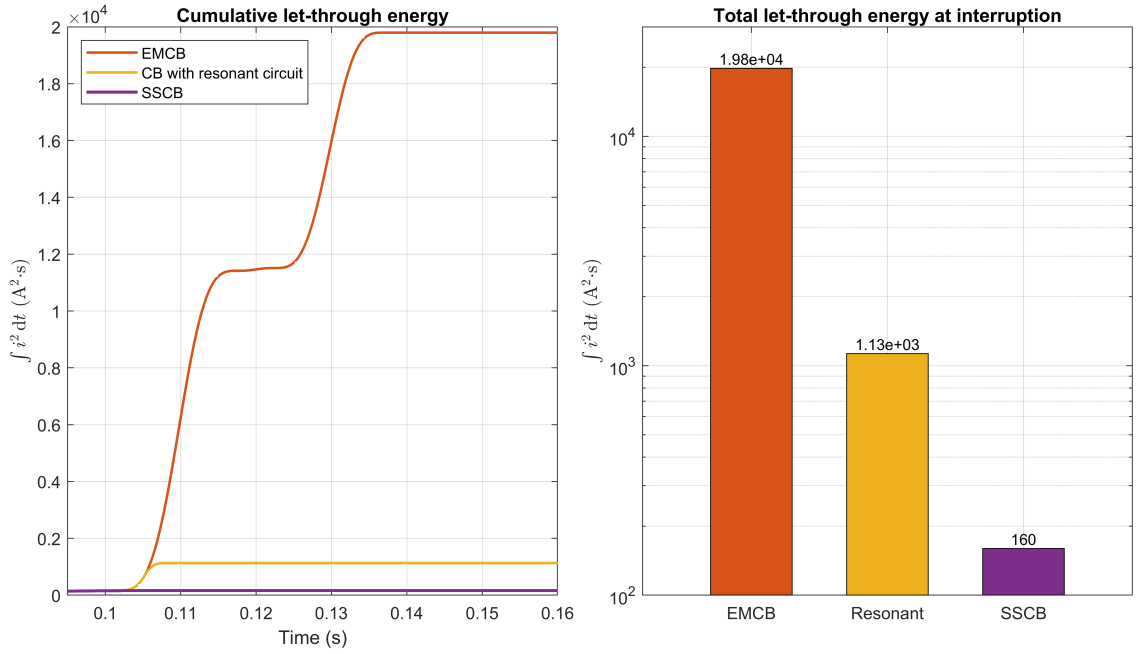


Figure 7.13. Cumulative let-through energy $\int i^2\,\mathrm{d}t$ for the four cases of Figure 7.12. The solid-state breaker caps the let-through energy at a negligible value; the resonant breaker accumulates a moderate amount before forced commutation; the electromechanical breaker and the uninterrupted case follow the same steeply-rising curve until the EMCB finally clears, by which point the accumulated I^2t is several orders of magnitude above that of the SSCB.

ical breakers and is substantially shorter even than that of resonant-assisted breakers, which directly translates into a much lower peak let-through current—and, more importantly, into a let-through energy that is lower by orders of magnitude, and therefore into a correspondingly lower thermal and mechanical stress on the protected equipment.

7.2 Three-phase distribution network

The single-phase study of Section 7.1 validated the operating principle of the breaker and of its control system in the simplest possible setting, in which the topology of the network plays no role and the breaker is exercised against a single, idealized fault. To assess the behavior of the breaker in a setting that is representative of a real distribution system, the analysis is now extended to a complete three-phase medium-voltage feeder, modeled in MATLAB/Simulink with the Simscape Electrical library.

The network used for this purpose is inspired by the radial distribution feeder studied by Tsimtsios and Nikolaidis [4], which is based on typical data of the Greek 20 kV distribution system. That feeder is attractive as a test network for the present work for two reasons. First, it is realistic: its main trunk is built from overhead lines of progressively smaller conductor cross-section as the distance from the substation increases, and its laterals use a still smaller cross-section, so that the network is genuinely *inhomogeneous* in its impedance data, exactly as a real feeder is. Second, it is a network in which the integration of distributed generation (DG) and the associated protection

issues have already been studied in the literature, which makes it a natural vehicle for examining how a solid-state circuit breaker behaves when it is installed in such a feeder—both when the feeder is purely passive and when it hosts a local synchronous generator. This section describes the model in detail; the simulation results follow in Sections 7.2.2 and 7.2.3.

7.2.1 Network description

The single-line diagram of the modeled network is shown in Figure 7.14. An external 150 kV transmission grid supplies, through a 150/20 kV bulk distribution transformer, a radial 20 kV, 50 Hz overhead feeder. The feeder consists of a main trunk, divided into four segments (L_{01}, L_{12}, L_{23}, L_{34}) that define the buses B_1 to B_4, and of four laterals (L_1 to L_4) that tap off the trunk at these buses and each terminate in a load. A local synchronous generator—representing a dispatchable DG unit such as a small biomass or hydro plant—is connected to the trunk through a dedicated step-up transformer.

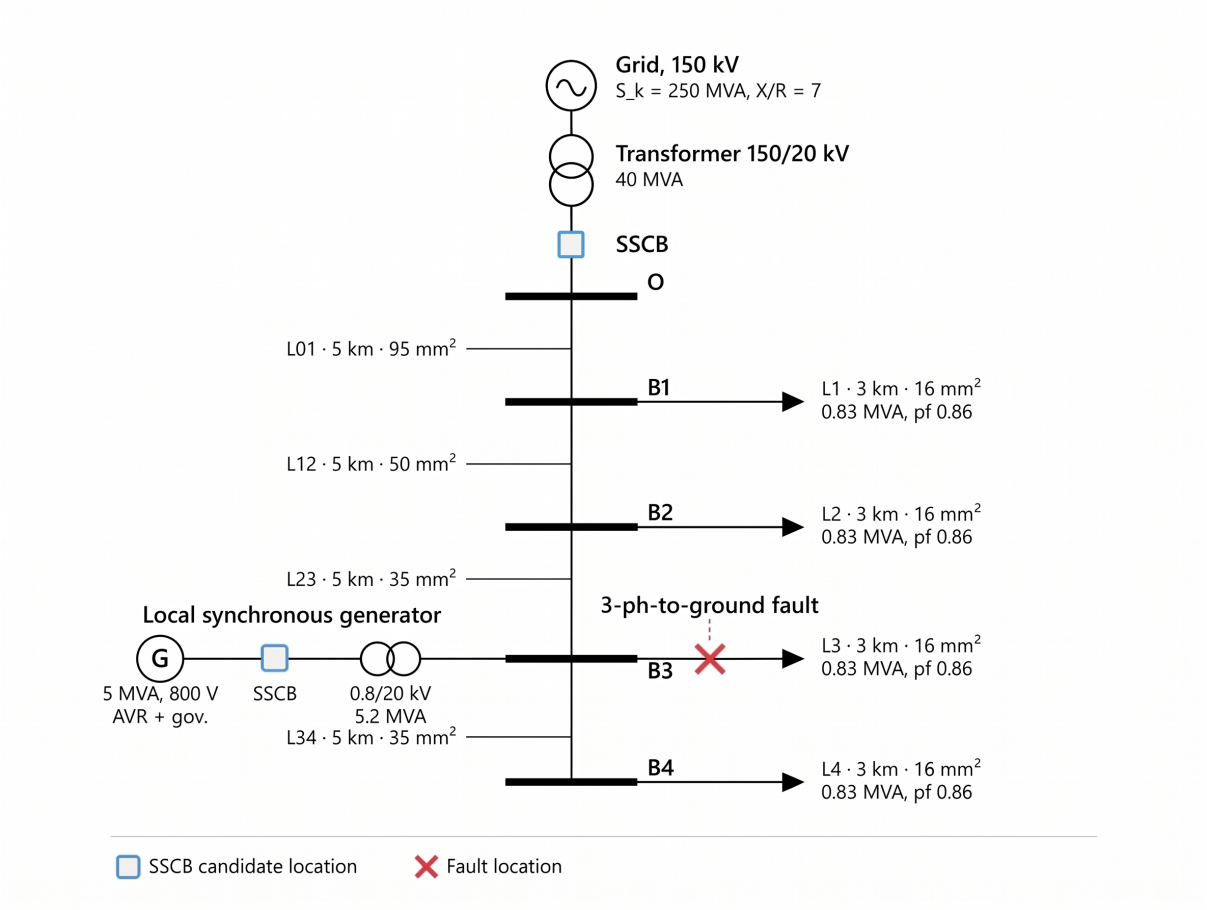


Figure 7.14. Single-line diagram of the modeled three-phase 20 kV *distribution feeder, with the two candidate locations for the installation of a solid-state circuit breaker.*

External grid and transformers. The upstream 150 kV network is represented by an equivalent three-phase voltage source behind its short-circuit impedance, with a short-circuit power of 250 MVA and an X/R ratio of 7. It feeds the feeder through a 40 MVA,

150/20 kV two-winding transformer. The local generator is connected to the 20 kV trunk through a 5.2 MVA, 0.8/20 kV step-up transformer. The ratings of the two transformers are summarized in Table 7.4.

Table 7.4. Parameters of the two transformers of the three-phase model.

Parameter	**Bulk transformer**	**Generator step-up**
Rated power S_n	40 MVA	5.2 MVA
Voltage ratio	150/20 kV	0.8/20 kV
Connection	Yg–Yg	Yg–Yg
Winding resistance (p.u.)	0.0025 per winding	0.0025 per winding
Rated frequency	50 Hz	50 Hz

Overhead lines. All line segments are modeled as lumped-parameter three-phase overhead lines. In accordance with the inhomogeneous character of the reference feeder [4], the trunk segments use conductors of decreasing cross-section as the distance from the substation increases, while the laterals use the smallest cross-section of all; this is reflected in the increasing per-kilometer series resistance of the segments. The lengths and the per-kilometer series parameters used for each line are given in Table 7.5, where R, L and M denote respectively the series resistance, the self-inductance and the mutual inductance per phase and per kilometer.

Table 7.5. Line segments of the three-phase feeder and their per-kilometer series parameters. The trunk segments L_{01}–L_{34} form the main feeder ($\approx$ 95, 50, 35 and 35 mm^2 equivalent cross-sections), while L_1–L_4 are the laterals ($\approx$ 16 mm^2).

Line	**Length** (km)	R (Ω/km)	L (mH/km)	M (mH/km)
L_{01}	5	0.2643	2.360	1.297
L_{12}	5	0.4533	2.500	1.271
L_{23}	5	0.6253	2.535	1.271
L_{34}	5	0.6253	2.535	1.271
L_1	3	1.3173	2.611	1.271
L_2	3	1.3173	2.611	1.271
L_3	3	1.3173	2.611	1.271
L_4	3	1.3173	2.611	1.271

The reference feeder is described in [4] by means of the positive- and zero-sequence series impedances Z_1 and Z_0 of each conductor type, rather than by the phase-domain parameters required by the lumped-parameter line block of the simulation library. The values of Table 7.5 were therefore obtained from the published sequence impedances by means of the standard transformation for a balanced three-phase line, in which the

per-phase self- and mutual inductances are related to the sequence inductances by

$$L_1 = L - M, \qquad L_0 = L + 2M, \tag{7.1}$$

where L is the phase self-inductance and M the mutual inductance between phases. Inverting these relations gives $L = (L_0 + 2L_1)/3$ and $M = (L_0 - L_1)/3$, which, together with the series resistance, are the quantities entered in the model. With the values of Table 7.5 this transformation reproduces the positive- and zero-sequence reactances of the reference feeder to within rounding, which confirms that the inhomogeneous character of the original line—and in particular the increase of the zero-sequence relative to the positive-sequence impedance as the conductor cross-section decreases—is faithfully preserved in the phase-domain model.

Loads. Each lateral terminates in a three-phase load, modeled as a series resistive–inductive branch of $R = 415\,\Omega$ and $L = 0.779\,\mathrm{H}$ per phase. At the nominal phase-to-phase voltage of 20 kV this corresponds to a moderate, lagging power factor load, so that the feeder operates under realistic loading conditions before the fault is applied.

Local synchronous generator. The DG unit is modeled by a standard round-rotor synchronous machine, rated at 5 MVA, 800 V, 50 Hz, with a single pole pair. Its principal parameters are listed in Table 7.6. The machine is initialized as the swing source of the local subsystem, delivering an active power of 3 MW at unity power factor before the fault. Unlike a converter-interfaced source, a directly-connected synchronous generator contributes a substantial short-circuit current and possesses real mechanical inertia; both of these properties are essential for the study of Section 7.2.3, in which the interaction between the breaker and the generator is examined.

The generator is equipped with the two control loops that a real unit would have, and which are the reason this configuration is of interest for the present study:

- an **automatic voltage regulator (AVR)** with an exciter of the standard IEEE Type AC1C alternator-rectifier type, which regulates the terminal voltage of the machine by acting on the field voltage. During a nearby fault the terminal voltage collapses, and the AVR responds by driving the field voltage towards its ceiling in an attempt to support the voltage; the speed with which the fault is cleared therefore directly affects the excursion that the excitation system undergoes.
- a **speed governor and prime mover**, modeled as a speed-droop governor acting on a first-order prime-mover (turbine) model. The governor regulates the mechanical power as a function of the rotor speed deviation, with a steady-state droop characteristic. Because the electrical torque of the machine drops sharply during a fault while the mechanical input cannot change instantaneously, the rotor accelerates; the resulting speed and power swing, and how quickly it is arrested, again depend strongly on the fault-clearing time.

The numerical settings of the governor (speed droop, governor time constant T_G and turbine time constant T_{CH}) and of the excitation system are summarized in Table 7.7. The excitation system is a standard IEEE Type AC1C alternator-rectifier exciter, with a

Table 7.6. Parameters of the local synchronous generator (round-rotor, standard parameterization).

Group	Parameter	Value
Ratings	Rated power S_n	5 MVA
	Rated voltage (line)	800 V
	Rated frequency	50 Hz
	Pole pairs	1
	Inertia constant H	3.525 s
Reactances (p.u.)	Synchronous X_d / X_q	1.81 / 1.76
	Transient X'_d / X'_q	0.30 / 0.65
	Subtransient X''_d / X''_q	0.23 / 0.25
	Leakage / zero-sequence X_l / X_0	0.15 / 0.15
	Armature resistance R_a	0.003
Time constants (s)	T'_{d0} / T'_d	8.0 / 1.326
	T''_{d0} / T''_d	0.03 / 0.023
Operating point	Active power P_{t0}	3 MW
	Reactive power Q_{t0}	0 Mvar

voltage regulator ($K_A = 300$) and the usual rate (derivative) feedback for stability; its output is limited so that the field voltage cannot exceed the exciter ceiling. The governor is a speed-droop governor with a 4 % droop acting on a non-reheat steam-turbine (first-order) prime-mover model, with the machine initially loaded to 0.6 p.u. of its rated torque.

Solid-state breaker and candidate locations. The breaker used in the three-phase model is the three-phase extension of the power stage validated in Section 7.1: each phase is interrupted by a back-to-back pair of power MOSFETs (on-state resistance 1 mΩ per device), and a metal-oxide varistor across each pole absorbs the inductive energy of the network at interruption and clamps the pole voltage. The three poles are commanded simultaneously by the same control logic described in Section 7.1.3, so that a fault detected on any phase disconnects all three.

Because a solid-state breaker is considerably more expensive than a conventional one, it is not realistic to install one on every line of the feeder; the more meaningful engineering question is *where* a single such device brings the greatest benefit. Following the same reasoning as in the CIGRE study of a comparable Greek feeder [44], two candidate locations are considered in this work and are marked in Figure 7.14:

- immediately **downstream of the** 150/20 kV **transformer**, at the head of the feeder, where the breaker sees the full fault current supplied by the upstream grid; and
- immediately **at the terminals of the local generator** (on the low-voltage, 800 V side of its step-up transformer), where the breaker protects the generator itself and limits the contribution that the machine makes to a fault elsewhere in the feeder.

Table 7.7. Settings of the generator control loops, as taken from the Simulink model. The excitation system follows the IEEE Type AC1C model.

Loop	Parameter	Value
Governor	Speed droop	4 %
	Governor time constant T_G	0.2 s
	Speed reference	1.0 p.u.
	Load reference setpoint	0.6 p.u.
Prime mover	Turbine time constant T_{CH}	0.3 s
	Initial torque	0.6 p.u.
AVR / exciter	Regulator gain K_A	300
(IEEE AC1C)	Regulator time constant T_A	0.01 s
	Rate feedback gain K_F	0.03
	Rate feedback time constant T_F	1 s
	Exciter constant K_E / time const. T_E	1 / 0.05 s
	Regulator output limits $V_{A,\max\,/\,\min}$	$\pm$14.5
	Field-voltage ceiling $E_{FE,\max}$	6.03 p.u.
	Initial field voltage E_{FD0}	1.4 p.u.

The two configurations expose different aspects of the breaker's behavior and are used in the following sections accordingly.

Feasibility of the two locations with present-day devices. The two locations are not equally realizable with the power semiconductors available today, and it is important to state this explicitly before the results are discussed. The generator-side location operates at the 800 V terminal voltage of the machine, i.e. in the low-voltage domain. A back-to-back pair of commercially mature SiC MOSFETs—of the same kind as the device used in the single-phase model of Section 7.1, in the 1.2 kV rating class appropriate to an 800 V system—comfortably blocks the system voltage, so a solid-state breaker at this point can be assembled from off-the-shelf components and is representative of the low-voltage SSCBs that are already reaching the market.

The head-of-feeder location, by contrast, sits on the 20 kV side of the bulk transformer. As the energy-absorption analysis of Section 7.2.2 shows, each pole is clamped at about 21 kV (approximately 1.3 times the peak phase-to-ground voltage), so every pole must block on the order of 20 kV in steady state and survive the clamping excursion at the instant of interruption. This is far beyond the rating of any single power device presently on the market: commercial SiC MOSFETs currently extend to about 3.3 kV, with 6.5 kV modules only beginning to appear, while devices in the 10–15 kV range remain laboratory demonstrators. A 20 kV pole therefore requires several such devices to be connected in series, with the attendant difficulty of ensuring static and dynamic voltage sharing—an approach that to date has been realized only in research prototypes and pilot demonstrators (predominantly for medium-voltage DC systems) rather than

as a mature, commercially available product for AC distribution.

For this reason, the head-of-feeder (20 kV) configuration should be read as a deliberately *theoretical*, forward-looking case. It is retained because it cleanly exposes effects that appear only at the head of the feeder—in particular the unequal energy loading of the three pole varistors analyzed in Section 7.2.2—and because it indicates the benefit that a medium-voltage SSCB would bring once the device technology matures; it is *not* included on the premise that such a breaker can be procured and installed at 20 kV with today's components. The generator-side (800 V) configuration, on the other hand, is realizable now, and it is on this configuration that the central, quantitative conclusions of the chapter (Section 7.2.3) rest.

Fault scenario. Unless otherwise stated, the disturbance applied to the network is a solid three-phase-to-ground fault with a fault resistance of 1 mΩ. The fault is applied at $t = 3.8$ s—that is, well after the initial electromagnetic and electromechanical transients of the model have settled and the generator has reached its steady operating point—and would persist for 1 s if it were not cleared. This late application instant is deliberate: it ensures that the pre-fault waveforms shown in the results represent a true steady state, against which the effect of the fault and of its interruption can be read unambiguously.

7.2.2 Grid-feeding configuration with passive loads

In the first configuration the local generator is left out of service, so that the feeder is supplied solely by the upstream 150 kV grid through the bulk transformer, and the solid-state breaker is placed at the head of the feeder—the 20 kV, forward-looking location whose practical status was discussed above. Although, as established there, a 20 kV pole cannot be built from a single present-day device, this configuration is retained deliberately and examined first, for two complementary reasons. As the three-phase counterpart of the single-phase study of Section 7.1, it confirms that the breaker and its control logic operate correctly when extended to three phases, before the more demanding case with a rotating machine is considered; and, being placed at the point of highest fault current in the network, it is the configuration that most clearly exposes an effect which is genuinely three-phase in nature and which has a direct bearing on device sizing—the unequal energy loading of the three pole varistors, analyzed below. It is precisely because this effect is most pronounced at the head of the feeder that the otherwise theoretical location earns its place in the analysis. As in the single-phase study, two interruption modes are examined—a direct interruption and an interruption with current limiting.

The direct-interruption case is shown in Figure 7.15. Before the fault, the three line currents form a balanced sinusoidal set and the bus voltages are at their nominal value. When the three-phase-to-ground fault is applied at $t = 3.8$ s, the currents in all three phases begin to rise; as soon as the current of any phase crosses the detection threshold, the control logic commands all three poles off, and the line currents are driven to zero within a fraction of a millisecond, exactly as in the single-phase case. One feature that is specific to the three-phase system is worth noting: because the three phases

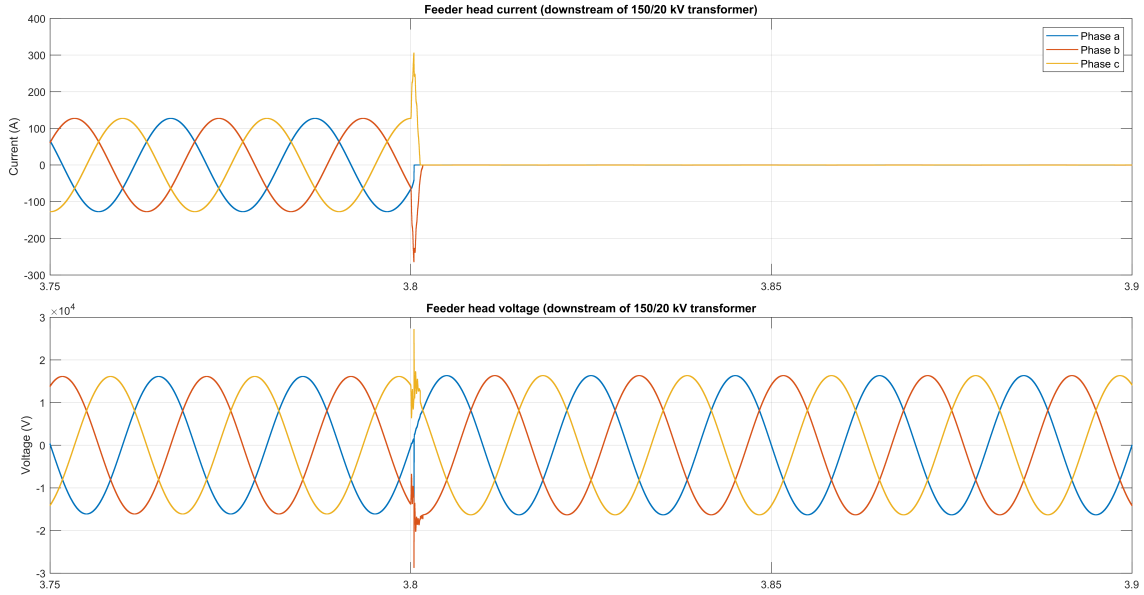


Figure 7.15. Grid-feeding configuration, direct interruption: three-phase line currents (top) and bus voltages (bottom) for a three-phase-to-ground fault cleared by the head-end SSCB.

are at different points of their cycle at the instant of interruption, the instantaneous current—and therefore the energy that each pole varistor must absorb—differs from phase to phase, the most heavily loaded pole being the one closest to its current peak when the breaker trips.

Unequal loading of the three pole varistors. The remark made above—that the energy each pole has to absorb at interruption is not the same on all three phases—can be made explicit by inspecting the voltage developed across the three metal-oxide varistors, one per pole, of the head-end breaker. These voltages are shown in Figure 7.16 for the same direct-interruption event of Figure 7.15.

Each trace exhibits the same three-stage signature. Before the fault, while the breaker conducts, the pole voltage is essentially zero. At the instant of interruption ($t = 3.8\,\mathrm{s}$) the line inductance forces the current to remain continuous, so the interrupted current is momentarily diverted into the varistor; the latter responds by clamping at its protection level—set in the model to 21 kV per pole, i.e. approximately 1.3 times the peak phase-to-ground voltage of the 20 kV feeder—and holds that voltage for as long as it takes to drive the trapped current to zero. This is the short, flat-topped excursion visible on each trace. Once the pole current has reached zero the varistor returns to its high-resistance region and the voltage across the now-open pole settles into the power-frequency recovery voltage, a sinusoid of approximately 16.3 kV peak ($20\,\mathrm{kV} \cdot \sqrt{2}/\sqrt{3}$), which is simply the system phase-to-ground voltage and carries no significant energy into the device.

The key observation is that the clamping excursions are *not* identical on the three phases. Although the three poles receive a common trip command and therefore open simultaneously, the three phase currents are 120° apart in their cycle, so that at the trip instant each pole is interrupting a different instantaneous current. Three consequences follow, all of which are visible in Figure 7.16:

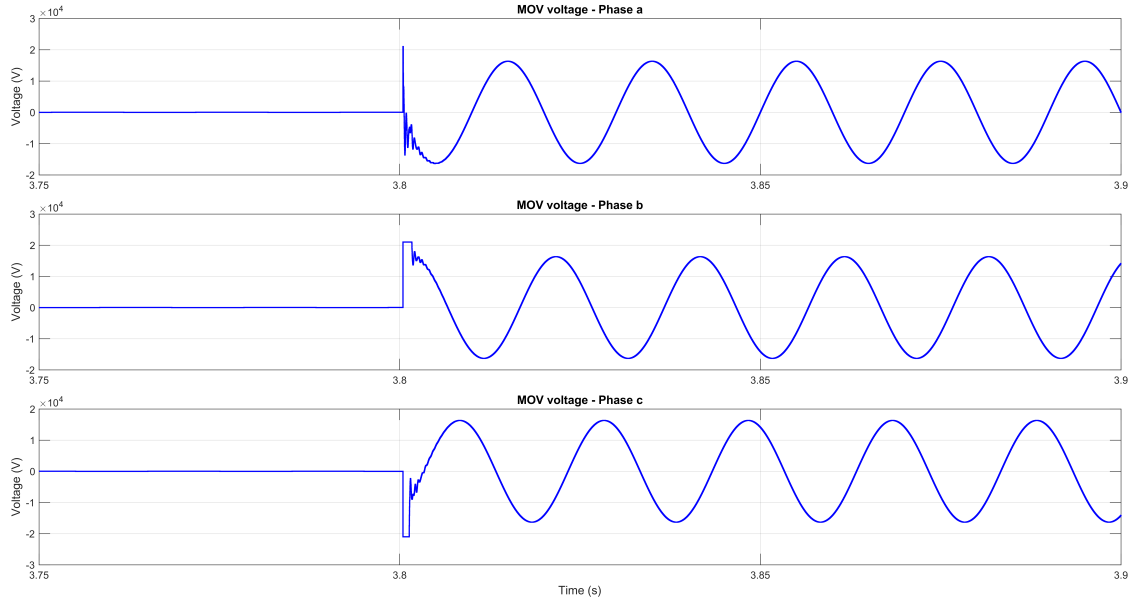


Figure 7.16. Voltage across the pole varistor of each phase (a: top, b: middle, c: bottom) of the head-end SSCB during the three-phase-to-ground fault, applied at $t = 3.8\,\mathrm{s}$. The brief, flat-topped spike at the instant of interruption is the MOV clamping *action, during which the varistor absorbs the trapped magnetic energy of the line; the steady sinusoid that follows is the power-frequency* recovery voltage *that now appears across the open pole, at which point the varistor is in its high-resistance region and dissipates essentially no energy.*

- **Polarity.** The varistor develops the voltage required to oppose the decaying pole current, so the polarity of the clamping spike follows the sign of the current being interrupted—positive on phases *a* and *b* and negative on phase *c* in this particular event.
- **Duration.** The clamp persists until the trapped magnetic energy of the pole has been dissipated; the larger the current at the trip instant, the longer this takes, which is why the clamping plateaux differ in width from phase to phase.
- **Energy.** The energy actually absorbed by a pole is $W = \int v_{\mathrm{MOV}}\, i_{\mathrm{MOV}}\, \mathrm{d}t$. Since the clamping voltage is practically the same on all three poles (it is fixed by the varistor characteristic), the energy is governed by the magnitude and duration of the interrupted current. The pole that is closest to its current peak when the breaker trips is therefore the one that absorbs the most energy—the *most heavily loaded pole* referred to above.

This has a concrete design implication. The point on the voltage cycle at which a fault occurs—and hence which phase happens to be near its current peak at the trip instant—is not under the designer's control and varies from one fault to the next. Over the population of possible fault instants, any of the three poles can be the most heavily stressed one. Each pole varistor (and the thermal capability of the associated semiconductor) must therefore be rated for the *worst-case single-phase* absorption energy rather than for the average across the three poles; sizing to the mean would leave the pole that happens to interrupt near its current peak under-rated.

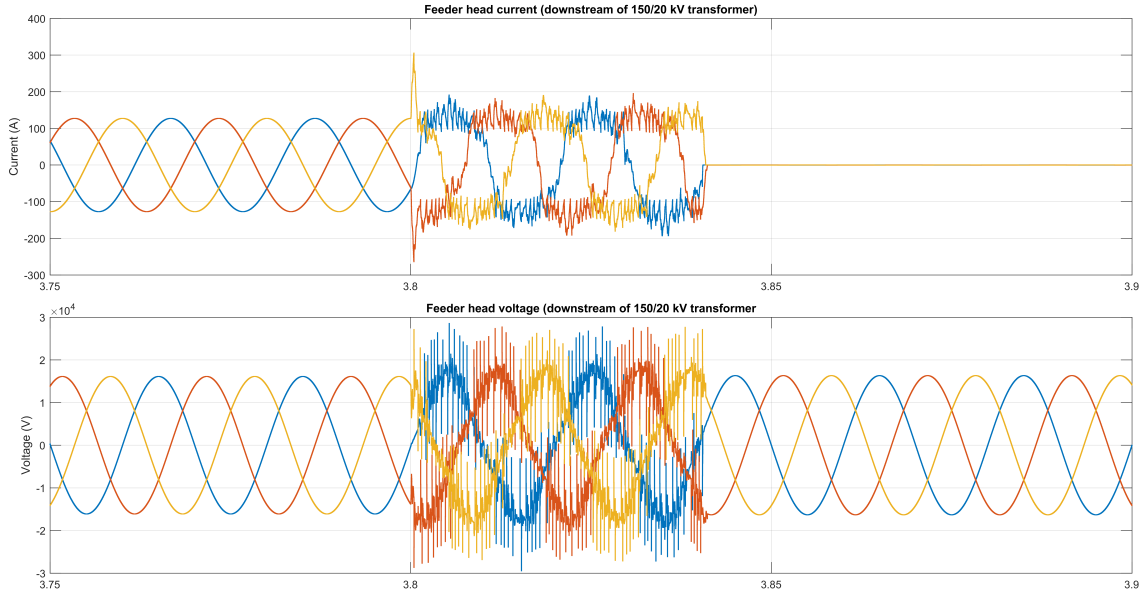


Figure 7.17. Grid-feeding configuration, interruption with current limiting: the line currents are held within the limiting band on all three phases before the definitive interruption.

When the current-limiting function is enabled (Figure 7.17), the breaker holds the line currents within the prescribed band on all three phases for the duration of the limiting window before performing the definitive interruption, reproducing on each phase the chopping behavior established for the single-phase case in Section 7.1.5. The three-phase results therefore confirm that the breaker behaves as designed in a balanced three-phase setting, and that the single-phase conclusions regarding the trade-off between let-through current and switching activity carry over directly to the three-phase case.

7.2.3 Configuration with a local synchronous generator

The configuration with the local synchronous generator is the central case of this chapter, because it exposes a phenomenon that neither the single-phase study nor a purely passive network can reveal: the interaction between the fault-clearing speed of the breaker and the electromechanical dynamics of a directly-connected rotating machine equipped with an automatic voltage regulator and a governor.

Scenario. The generator is now in service, delivering 3 MW to the feeder with its AVR and governor active, and the solid-state breaker ($SSCB_1$) is placed on the low-voltage (800 V) side of the generator step-up transformer, between the machine and the trunk—that is, it protects the generator branch rather than the head of the feeder. The disturbance is the standard three-phase-to-ground fault, applied this time at bus B_3 of the trunk, i.e. at a load bus some distance away from the generator rather than at its terminals. This arrangement reflects a realistic protection philosophy: the expensive solid-state device is dedicated to the generator, whose contribution it can interrupt very quickly, while the fault on the trunk continues to be fed by the upstream grid. In other

words, the role of SSCB_1 in this scenario is to *isolate and protect the generator*, not to clear the trunk fault itself; the latter would, in practice, be cleared by the feeder protection. The quantities of interest are therefore those internal to the generator: its stator current, its terminal voltage, the field voltage commanded by the AVR, and the rotor speed and electrical torque governed by the prime mover.

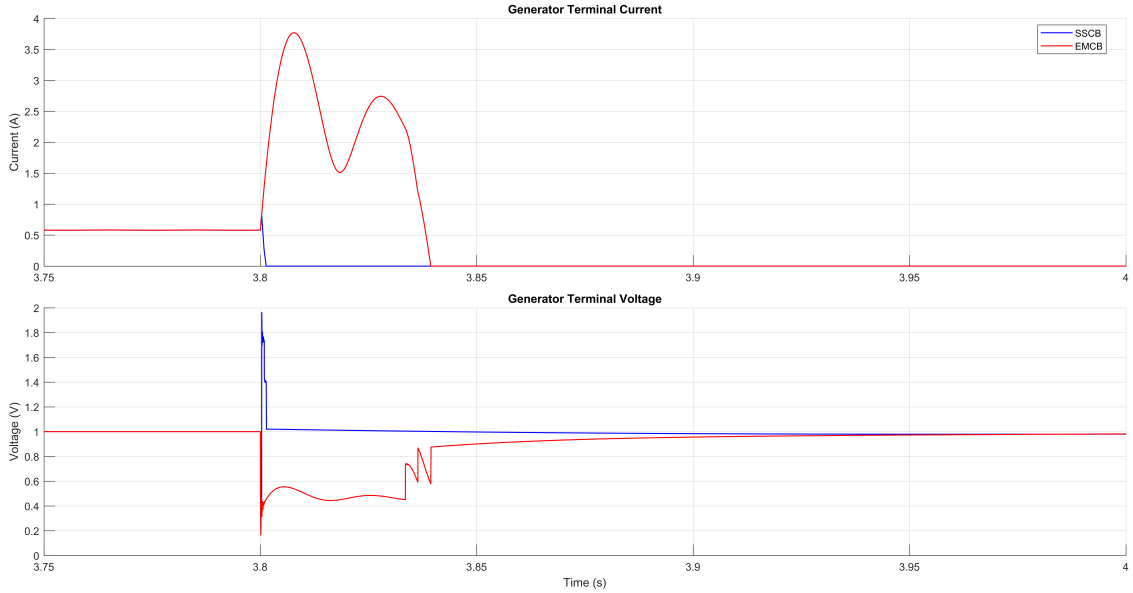


Figure 7.18. Response of the local generator to a fault at B_3: terminal current (top) and terminal voltage (bottom) for the solid-state breaker (blue) and the electromechanical breaker (red). The SSCB interrupts the fault current within a few milliseconds; the brief overvoltage spike immediately after interruption ($\approx$ 1.9 pu) is the recovery voltage across the now-open pole. With the EMCB the current reaches approximately six times its pre-fault value before being interrupted some 40 ms *after fault inception, and the terminal voltage remains depressed throughout.*

Response with the solid-state breaker. Figure 7.18 shows the terminal current and voltage of the generator for both interruption technologies. At the instant of the fault ($t = 3.8$ s) the terminal voltage collapses and the stator current begins to rise as the generator starts to feed the fault. With the solid-state breaker the current is driven to zero within a few milliseconds—before any of the electromechanical dynamics of the machine have time to develop. With the electromechanical breaker, by contrast, the current reaches approximately 3.75 pu, or roughly six times the pre-fault value, and is sustained for approximately 40 ms before the mechanical contacts part.

Recovery voltage at the generator terminals. Immediately after the solid-state breaker opens, the terminal voltage of the machine rises briefly to approximately 1.9 pu before settling at its no-load value. This transient overvoltage is the recovery voltage across the open pole: with the stator current forced to zero, the AVR—which had begun to drive the field voltage upward in response to the initial voltage collapse—now acts on an unloaded machine, causing a brief overshoot. The excursion is short-lived and well within the insulation capability of the machine; it is absent in the EMCB case because

the generator remains connected to the depressed network voltage for the full duration of the mechanical opening delay.

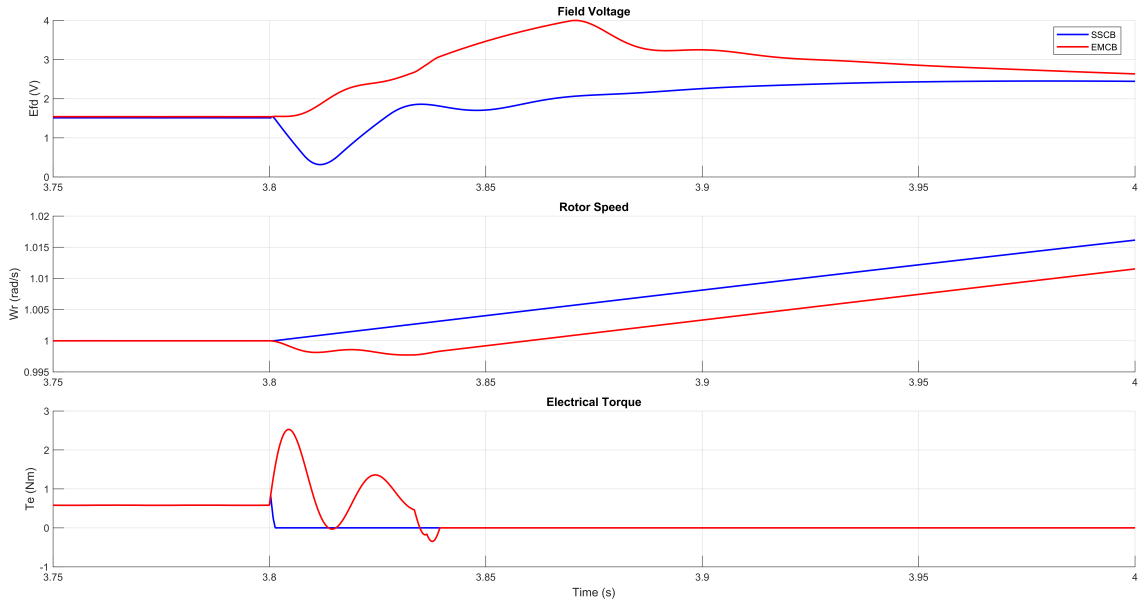


Figure 7.19. Comparison of the generator response for the solid-state breaker (blue) and the electromechanical breaker (red): field voltage E_{fd} (top), rotor speed ω_r (middle) and electrical torque T_e (bottom), for a three-phase-to-ground fault at bus B_3 applied at $t = 3.8\,\mathrm{s}$. With the EMCB the field voltage reaches approximately 2.7 times its initial value and the electrical torque oscillates violently between -0.5 and $+2.5\,\mathrm{pu}$; with the SSCB neither excursion develops.

Comparison with a slower breaker. Figure 7.19 overlays the field voltage, rotor speed and electrical torque of the generator for the solid-state breaker and for the electromechanical breaker with a mechanical opening delay of approximately 40 ms. Three differences are immediately apparent.

First, the field voltage commanded by the AVR reaches approximately 2.7 times its pre-fault value with the electromechanical breaker, as the regulator attempts to restore the collapsed terminal voltage over the full duration of the fault; with the solid-state breaker the field voltage dips briefly at the instant of interruption—a consequence of the instantaneous current interruption—and then rises gently as the AVR regulates the unloaded machine back to its set-point. The excursion is negligible compared with that produced by the electromechanical breaker.

Second, the electrical torque oscillates between approximately -0.5 and $+2.5\,\mathrm{pu}$ with the electromechanical breaker, imposing a significant cyclic mechanical stress on the generator shaft during the fault interval. With the solid-state breaker the torque drops cleanly to zero within microseconds of the trip command and remains there, so that the shaft is subjected to no oscillatory loading whatsoever.

Third, the rotor speed deviation, though small in both cases over the $t = 4\,\mathrm{s}$ window shown—a direct consequence of the large inertia constant $H = 3.525\,\mathrm{s}$ of the machine—develops differently in the two cases. With the electromechanical breaker the rotor first decelerates slightly during the fault (the electrical torque momentarily exceeds

the mechanical input) before accelerating after interruption, producing a characteristic swing in the speed trace. With the solid-state breaker only a monotonic, slow acceleration is observed after the trip, driven by the governor's gradual response to the loss of electrical load; no speed swing occurs because the fault is cleared before the electromechanical dynamics can be excited.

Implication for renewable-energy hosting capacity. This result has a significance that extends beyond the protection of the individual machine. As discussed in Section 6.5.1, the fault current that a generator contributes to the network adds to the prospective short-circuit level, which is one of the binding constraints on how much distributed generation a feeder can host. The simulations above show, at the level of a single unit, how fast interruption shortens the duration of the generator's fault-current contribution; current limiting can additionally bound the current that passes through the protected branch. This reduces actual let-through stress, but does not by itself reduce the prospective short-circuit level calculated without the limiting device. Any claimed hosting-capacity benefit requires a network-level assessment of equipment withstand and protection coordination, as motivated by studies of comparable Greek distribution networks [44]. In particular, immediate disconnection for an external fault may conflict with applicable LVRT requirements [3]; the present generator study is a protection comparison, not a demonstration of connection-code compliance.

Chapter 8

Experimental Validation

The analysis presented in the previous chapters is based on theoretical considerations and, for the SSCB topologies of Chapter 6, on simulation studies. In order to complement this analysis with a first assessment against real hardware, a set of laboratory experiments was carried out on a commercially available SSCB evaluation platform. This chapter describes the experimental setup that was used and presents the tests that were performed, together with the corresponding oscilloscope and simulation captures.

8.1 Experimental setup

The experimental setup consists of three main elements: the SSCB device under test, a programmable electronic load that emulates the protected circuit and allows the current to be set and varied in a controlled manner, and a control stage that commands the turn-on and turn-off (trip) of the SSCB. Two different control paths were used in the course of the experiments: the manual control switches provided on the evaluation board itself, and an external, processor-based controller built around a Texas Instruments LaunchPad. The AC supply for the tests was obtained from a variable-voltage autotransformer (Variac), set to approximately $65\,V_{rms}$ – the value measured directly across the open contacts in the comparison test of Section 8.2.5 – and a digital oscilloscope was used throughout to capture the relevant voltage and current waveforms. Figure 8.1 identifies the main components of the laboratory bench, while Figure 8.2 summarizes its power, control and measurement connections, including the parallel-board configuration.

8.1.1 onsemi Combo JFET SSCB evaluation board

The device under test is the onsemi *Combo JFET SSCB Evaluation Board* (EVBUM2926/D) [12], built around the UG4SC075005L8S Combo JFET device in a TOLL package. A Combo JFET is a composite power device that integrates a low-voltage silicon MOSFET in series with a high-voltage, normally-on silicon-carbide (SiC) JFET. Unlike a conventional cascode arrangement, in which the JFET gate is permanently tied to the source of the low-voltage MOSFET, the Combo JFET brings out both gates – the MOSFET gate and the JFET gate – as separate, independently accessible terminals. This additional degree of freedom is exploited on the evaluation board to over-drive the JFET gate in order to reduce the effective on-state resistance, to control the switching speed independently of the low-voltage stage, and to sense the JFET junction temperature indirectly through its gate-to-source voltage, while the device retains the normally-off behavior of a standard cascode switch.

The power stage of the board is bidirectional, as required for an AC application: it is built from four identical power cells, each containing a Combo JFET together with its own gate-drive resistors and a blocking diode, arranged as two JFETs in parallel per

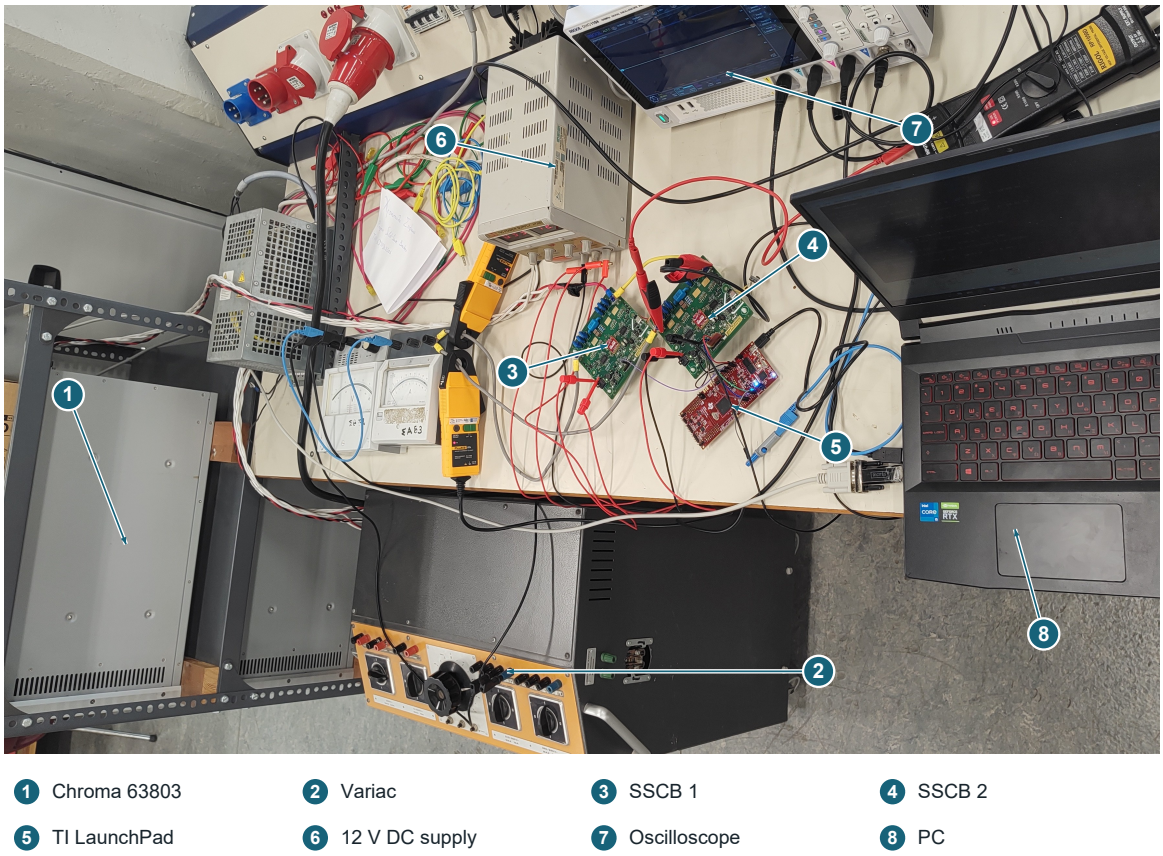
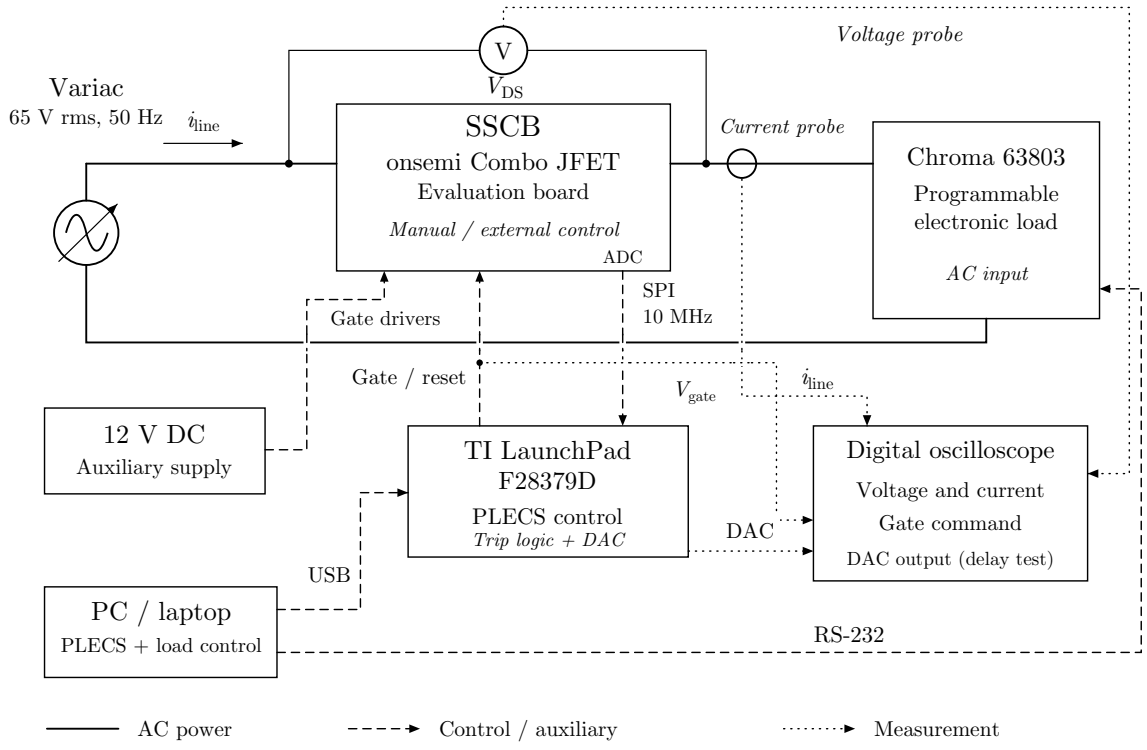


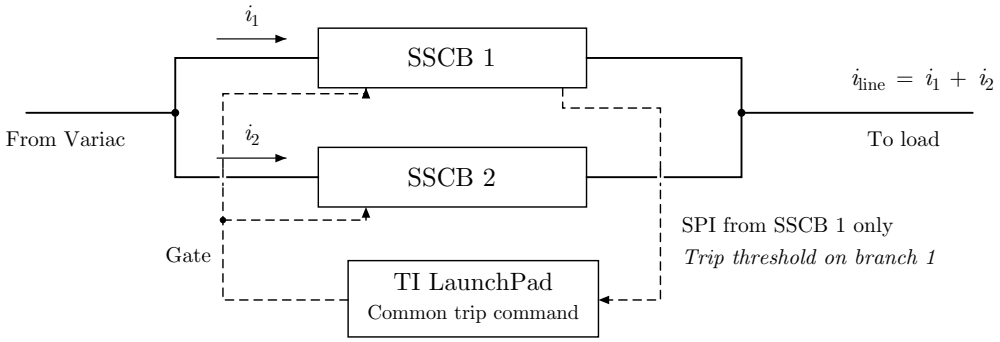
Figure 8.1. Laboratory setup in the parallel-board configuration: (1) Chroma 63803 electronic load; (2) Variac; (3–4) SSCB evaluation boards; (5) Texas Instruments LaunchPad F28379D; (6) 12 V DC auxiliary supply; (7) digital oscilloscope; (8) control PC.

polarity connected in a common-source series configuration. RC snubbers, a transient-voltage-suppressor (TVS) diode and metal-oxide varistors (MOVs) are placed across the power stage to absorb the energy stored in stray inductances when the JFETs turn off. The current is measured with shunt resistors, and a hardware over-current comparator with an adjustable threshold latches the SSCB into the off state as soon as the current exceeds the configured limit, until it is reset either manually or through software. The drain-to-source voltage of each JFET pair is also monitored through a desaturation-sensing circuit, and the JFET junction temperature is estimated from the JFET gate-to-source voltage using a dedicated sensing and averaging circuit that removes the offset introduced by the low-voltage MOSFET stage. Onboard control and telemetry are provided by a QPG6105 wireless system-on-chip, which also exposes a manual-control mode (through slide switches and a push button) and an external-access header that allows the gate-command and reset signals to be driven directly from external hardware. The board accepts power at its HV+ terminals over a range of 0–350 V AC or DC, with a continuous current rating of 10 A_{rms}.

(a) Laboratory setup



(b) Parallel-board experiment



Supply, load and measurement equipment are as in (a).

Figure 8.2. Schematic of the experimental setup: (a) single-board configuration, showing the Variac, SSCB evaluation board, programmable electronic load, auxiliary supply, LaunchPad controller, PC and oscilloscope; (b) parallel connection of two SSCB boards driven by a common gate command. In the parallel test, only the current of branch 1 is acquired over SPI and compared against the trip threshold. Line styles distinguish AC power, control/auxiliary and measurement connections.

8.1.2 Programmable electronic load

A programmable electronic load (a Chroma 63803 electronic load) was connected downstream of the SSCB to emulate the protected circuit and to provide a controlled, repeatable current for each test. The load was configured and operated from a PC over an RS-232 serial connection, which allowed the desired current level to be set programmatically before each run and kept constant for the duration of the test.

8.1.3 External control: Texas Instruments LaunchPad and PLECS

For the tests in which the SSCB had to be commanded by an external controller rather than by the manual switches or the onboard MCU of the evaluation board, a Texas Instruments LaunchPad F28379D development board was used. The control logic was implemented as a PLECS model and downloaded to the LaunchPad using PLECS's automatic code-generation support for this target, so that the LaunchPad could drive the SSCB's external gate-command and reset lines in real time without any hand-written embedded code. As shown in Figure 8.3, the line current is acquired through the LaunchPad's SPI-connected ADC, scaled and offset-corrected, and compared against a programmable overcurrent threshold; a set–reset latch then holds the gate-command output low (tripped) once the threshold has been exceeded, until it is reset by the control script. In parallel, the reconstructed current is also written back out through the on-board DAC, which is what makes it possible to compare the digitally processed current against the current measured directly with a current probe, as described in Section 8.2.4.

Concretely, the line current is not read through the LaunchPad's own on-chip ADC. The onsemi board carries its own eight-channel, 16-bit analog-to-digital converter, which digitizes the output of the shunt-and-amplifier current-sensing stage described in Section 8.1.1, and the LaunchPad reads its conversions over a 10 MHz SPI link. Because SPI transfers data one byte at a time, each conversion arrives not as a single number but as three consecutive 8-bit words, and the first task of the PLECS model is simply to put them back together: the three words are weighted by 2^{12}, 2^{4} and 2^{-4} and summed, which restores each byte to its proper bit position within the frame. This reassembly is arithmetic bookkeeping rather than scaling – it is equivalent to the ordinary big-endian concatenation of the two data bytes into the 16-bit conversion word, the third byte contributing less than one least-significant bit.

Only once the code has been reassembled does the conversion into physical units take place, in three distinct steps. First, the code is multiplied by $3.3\,\mathrm{V}/2^{20}$. The divisor is 2^{20} rather than 2^{16} because the weights above leave the reassembled code shifted four bits to the left of the 16-bit conversion word; the net effect is therefore to map that word onto the converter's 0–3.3 V input range, one least-significant bit corresponding to $3.3\,\mathrm{V}/2^{16} \approx 50\,\mu\mathrm{V}$. Second, the zero-current bias of the sensing stage, measured as 1.576 V, is subtracted. This step is necessary because the line current is alternating and therefore takes both signs, whereas the converter accepts only positive voltages: the sensing stage consequently places zero current near the middle of the

input range, and that offset must be removed before the sign of the current can be recovered. Third, the result is multiplied by the sensitivity of the current-sensing stage, 74.12 A/V (equivalently, a shunt-and-amplifier gain of about 13.5 mV/A), which yields the instantaneous line current in amperes, with a resolution of about 3.7 mA and a measurable range of roughly ± 120 A – far wider than the 10 A_{rms} continuous rating of the board, as is necessary if fault currents are to be captured without saturating the measurement.

This reconstructed current is used directly by the overcurrent-detection logic of Figure 8.3, and, for the response-time measurements of Section 8.2.4, is separately rescaled and offset to fit the on-board DAC's unipolar 0–3.3 V output range before being written back out for comparison with the current probe.

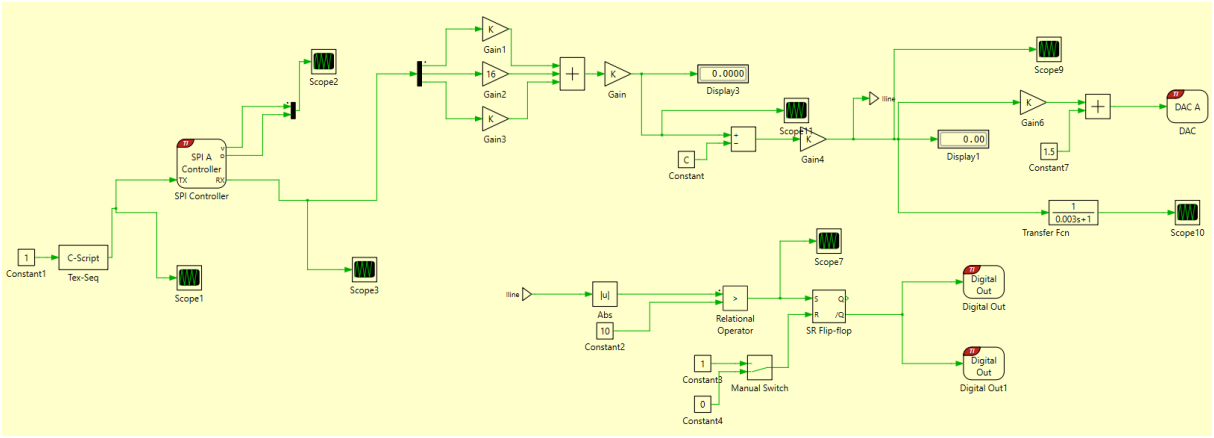


Figure 8.3. PLECS model of the control algorithm downloaded to the Texas Instruments LaunchPad: SPI-based acquisition and scaling of the line current, overcurrent detection through a set–reset latch that drives the digital gate-command outputs, and reconstruction of the acquired current through the on-board DAC for comparison with the directly measured current.

8.2 Experiments performed

Using the setup of Section 8.1, five experiments were carried out; they are presented in the following subsections together with the corresponding oscilloscope captures.

8.2.1 Interruption with a manual switch

As a first, baseline test, the SSCB was operated in its manual-control mode, in which the turn-on and turn-off (trip) commands are issued directly through the switches provided on the evaluation board rather than by an external controller. With the programmable load drawing a steady current of 10 A_{rms} from a 65 V_{rms} supply, the SSCB was manually commanded to interrupt the current, in order to confirm the basic conduction and interruption behavior of the board before proceeding to the more elaborate, processor-controlled tests.

The measurement is presented at two time scales. Figure 8.4 covers a window of approximately 100 ms, long enough for five complete cycles of the 50 Hz supply

to be seen, and therefore places the interruption in the context of normal operation; Figure 8.5 zooms into a window of roughly 320 μs around the switching instant, where the interruption transient itself becomes visible. The same convention – one capture showing the full sinusoid and one zoomed capture of the transient – is used for the experiments that follow.

In the wide view of Figure 8.4, the line current i_{line} is a clean sinusoid of approximately 14 A peak (corresponding to the 10 A_{rms} setting of the programmable load) for as long as the breaker conducts, while the drain-source voltage V_{DS} across the SSCB stays essentially at zero: in the on-state the device behaves as a closed switch and the whole supply voltage is dropped across the load. The gate-command voltage V_{gate} sits at its high level of about 3 V throughout this interval. At $t \approx -18.2$ ms the manual switch is actuated: V_{gate} steps to zero and the current is chopped essentially instantaneously, in the middle of a negative half-cycle and at close to its peak value, which is the most demanding instant at which an interruption can occur. After the trip the current remains at zero for the rest of the record while V_{DS} takes over the blocking duty, the low-amplitude residual oscillation visible on it afterwards being the source voltage divided between the open device and the remaining circuit impedance.

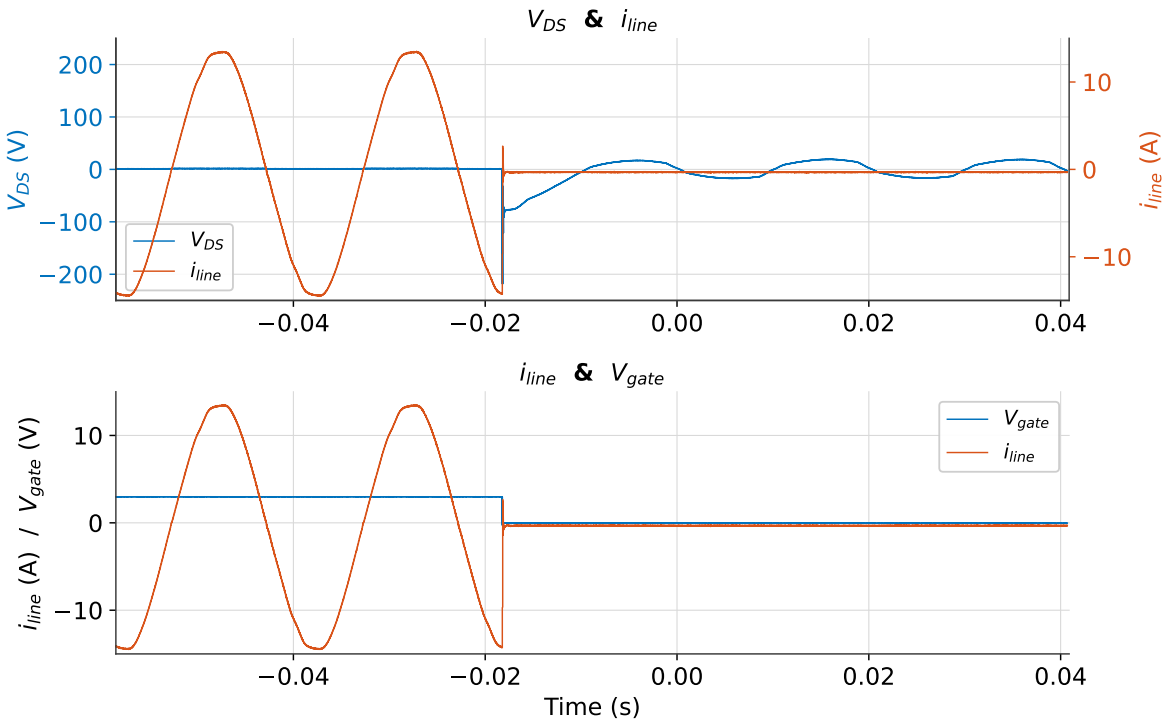


Figure 8.4. Interruption of the SSCB using the manual control switch ($V = 65\,V_{rms}$, $I = 10\,A_{rms}$), shown over several cycles of the supply: drain-source voltage and line current (top), line current and gate-command voltage (bottom).

The zoomed capture of Figure 8.5 resolves what happens during the switching transient itself, and three points are marked on it in order to separate the successive stages of the turn-off. Point (1), at $t = -18.1852$ ms, is the instant at which the gate command is withdrawn: V_{gate} collapses from its high level of 2.98 V to zero while the

line current is still flowing at $-14.20\,\mathrm{A}$, that is, essentially at the peak of a negative half-cycle. Point (2), at $t = -18.1547\,\mathrm{ms}$, is the instant at which the current first reaches zero. Point (3), at $t = -18.1021\,\mathrm{ms}$, marks the end of the transient. Because the current does not simply stop at its first zero but rings for some time afterwards, this instant is not judged by eye but taken as the last moment at which the current still departs from its final value by more than 5 % of the current that was interrupted. The same rule is applied to the processor-commanded interruption of Section 8.2.2, so that the two settling times can be compared directly.

The two intervals defined by these points therefore have distinct physical meanings, and both are marked directly on the figure:

- $\Delta t_1 = t_{(2)} - t_{(1)} = 30.5\,\mu\mathrm{s}$ is the time to the *first current zero*. It measures how long the device takes to force the line current down from its full instantaneous value to zero once the gate command has been removed, and it is the interval that determines the peak stress imposed on the breaker and the energy that the clamping branch has to absorb.
- $\Delta t_2 = t_{(3)} - t_{(1)} = 83.1\,\mu\mathrm{s}$ is the *settling time* of the interruption. After the first zero crossing the current overshoots to about $+2.7\,\mathrm{A}$ and then undershoots to roughly $-1.4\,\mathrm{A}$, ringing as the output capacitance of the device exchanges energy with the snubber network and the stray inductance of the loop. Only once this lightly damped oscillation has decayed is the circuit genuinely de-energized, so Δt_2 is the interval that should be quoted as the interruption time of the breaker.

The distinction matters in practice: quoting only Δt_1 would understate the interruption time by a factor of nearly three.

During the same transient the drain-source voltage, visible in the wide view of Figure 8.4, swings to $-218\,\mathrm{V}$, several times the peak of the supply. This happens because the stray inductance of the loop opposes the rapid change of current and its stored energy has to be diverted into the clamping and snubber network of the board. This overvoltage is precisely the phenomenon that makes the energy-absorption branch discussed in Chapter 6 indispensable in a solid-state breaker. Even on the most conservative reading, the interruption is already more than two orders of magnitude faster than that of the electromechanical contactor examined in Section 8.2.5.

8.2.2 Interruption using the Texas Instruments LaunchPad

In the second experiment, the trip command was instead issued by the external, PLECS-programmed LaunchPad controller described in Section 8.1.3, in place of the manual switch. With the programmable load set to $5\,\mathrm{A_{rms}}$, the software overcurrent threshold was configured to 11 A; a current excursion beyond this threshold was then produced and the resulting automatic trip was captured. This test verifies that the SSCB can be commanded reliably by an external, processor-based controller through its gate-command interface, which is the control path that would be used in a realistic protection application, in which the trip decision is taken by a protection relay or controller rather than by a human operator.

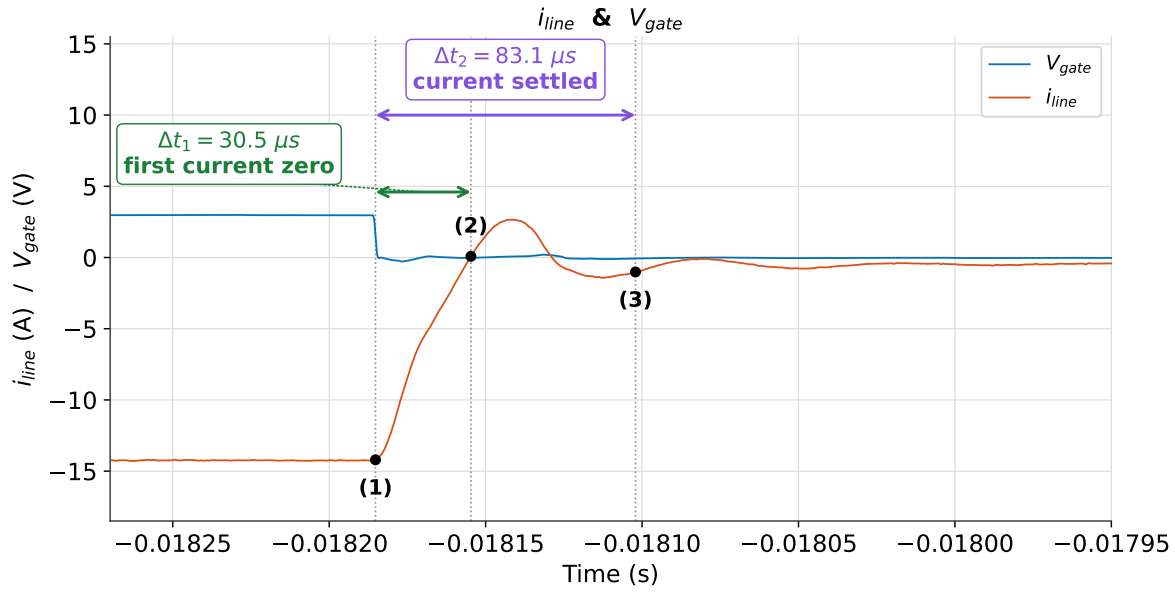


Figure 8.5. Zoomed view of the interruption of Figure 8.4 around the switching instant, showing the line current and the gate-command voltage. Point (1) is the withdrawal of the gate command, point (2) the first current zero and point (3) the instant at which the current has settled; $\Delta t_1 = 30.5\,\mu$s is therefore the time to the first current zero and $\Delta t_2 = 83.1\,\mu$s the settling time of the interruption.

Since what matters in this test is the relationship between the line current and the trip decision taken by the controller, only the line current i_{line} and the gate-command voltage V_{gate} are plotted. The drain-source voltage behaves exactly as already described in Section 8.2.1 and is omitted, so that the two signals which define the response of the protection loop can be shown on a single common axis and compared directly.

Figure 8.6 shows the event over a window of 80 ms, that is, four full cycles of the supply. For most of the record the current is a steady sinusoid and the gate command is held at its high level of approximately 3.2 V. Over the last cycle before the trip the load setting is increased and the envelope of the current can be seen to grow, until the instantaneous value touches the 11 A software threshold – drawn as a dashed line on the figure – at $t = 0$. At that instant the gate command drops to zero and the current is extinguished; for the remaining two cycles both traces stay flat, confirming that the breaker latches in the off state rather than attempting to re-close. The wide view also makes clear that the trip is triggered by the *instantaneous* value of the current crossing the threshold and not by an rms or averaged quantity, which is what allows the response to be as fast as it is.

Figure 8.7 zooms into a window of 360 μs around the trip, marked with the same three-point convention and the same settling rule used for the manual switch. Point (1) is the trip instant: the current reaches 11.00 A, the threshold is crossed and the gate command is withdrawn. Point (2), $\Delta t_1 = 19.6\,\mu$s later, is the first current zero, and point (3), $\Delta t_2 = 84.3\,\mu$s after the trip, is the instant at which the current has settled. As in the manual-switch test the current does not simply stop at the first zero: it undershoots to about -4.2 A and then rings with the snubber and the stray inductance of the loop

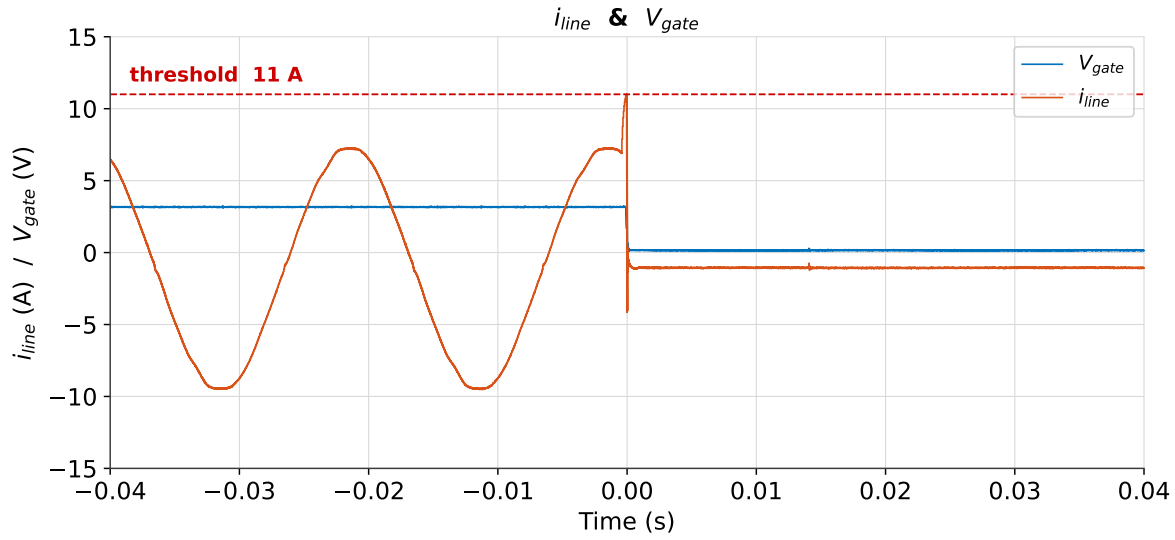


Figure 8.6. Interruption of the SSCB commanded by the Texas Instruments LaunchPad controller ($V = 65\,\mathrm{V_{rms}}$, $I = 5\,\mathrm{A_{rms}}$, software overcurrent threshold 11 A), shown over several cycles of the supply: line current and gate-command voltage. The dashed line marks the configured trip threshold.

before settling.

Comparing the two tests separates the two effects, and the comparison is only meaningful because the same settling rule has been applied to both. The first current zero is reached in 19.6 μs here against 30.5 μs for the manual switch, consistent with the smaller current being interrupted in this case (11.0 A against 14.2 A). The settling times, on the other hand, are practically identical: 84.3 μs against 83.1 μs, a difference of under one and a half percent. This is the result one should expect on physical grounds: the ringing that follows the current zero is governed by the output capacitance of the device together with the snubber network and the stray inductance of the loop, and none of these change between the two tests – the same board, in the same physical arrangement, is being switched. What changes is only *how* the turn-off is commanded, and the measurement confirms that this makes no difference to the decay of the transient.

The essential conclusion, therefore, is that replacing the human operator with a processor-based controller does not degrade the interruption at all: the complete detection-to-interruption path remains well inside a millisecond and the turn-off dynamics are unchanged. The latency that the digital chain itself contributes to the overall response is isolated and quantified separately in Section 8.2.4.

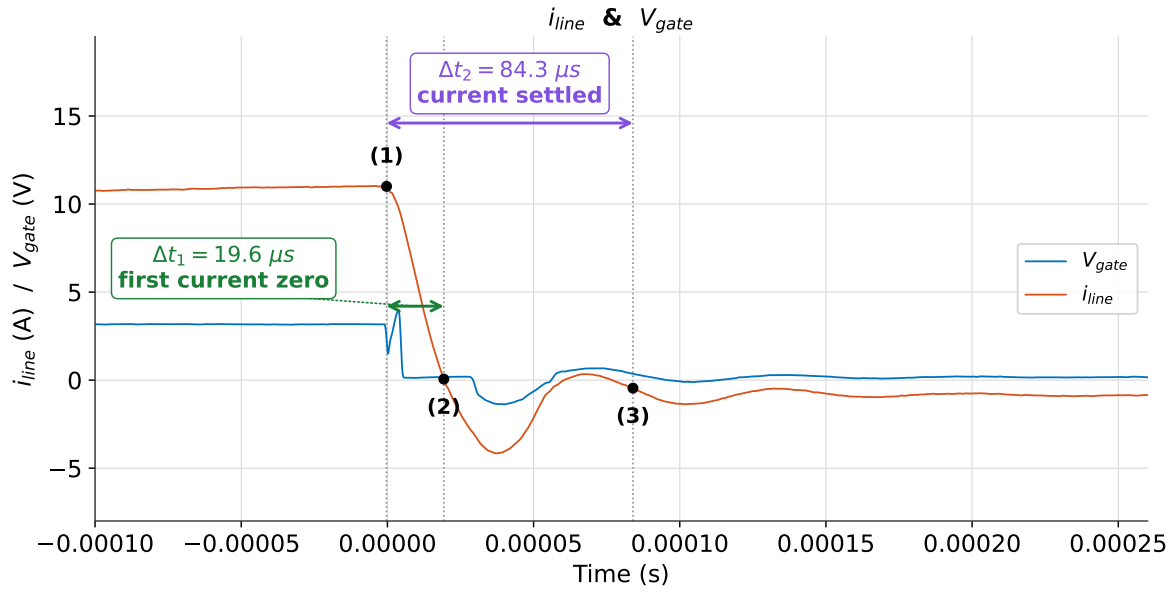


Figure 8.7. Zoomed view of the trip of Figure 8.6, showing the line current and the gate-command voltage. Point (1) is the crossing of the 11 A *threshold and the withdrawal of the gate command, point (2) the first current zero ($\Delta t_1 = 19.6\,\mu$s) and point (3) the instant at which the current has settled ($\Delta t_2 = 84.3\,\mu$s), determined with the same rule as in Figure 8.5.*

8.2.3 Parallel operation of two SSCB units

Realizing SSCBs for current ratings higher than a single commercial module can support typically requires the parallel connection of several units, which raises the question of current sharing between the parallel branches. In this experiment, two evaluation boards were connected in parallel – the same two boards visible side by side on the bench in Figure 8.1 – and driven by a common gate command issued by the LaunchPad controller, so that both units would be commanded to turn off simultaneously. With the programmable load set to 12 A_{rms} and the software overcurrent threshold set to 10 A, the combined conduction and interruption behavior of the two units was recorded in order to assess how evenly the load current is shared between them.

It is worth being explicit about how the trip decision is taken here, because the threshold is not compared against the total line current. The LaunchPad samples the current of *one* of the two breakers only, and issues the common gate command as soon as that single measurement exceeds the configured limit. Since each unit carries approximately half of the load, a 10 A threshold on one branch corresponds to roughly 20 A of total instantaneous line current. This is why the arrangement conducts for several cycles at a branch peak of about 8.5 A without tripping, and fires only once the load is raised far enough for the monitored branch to reach the limit – which is what the capture shows, the last half-cycle before the trip peaking at −9.95 A on that branch against the 8.5 A of the preceding ones.

As in the previous test, only the two branch currents $i_{line,1}$ and $i_{line,2}$ and the common gate command V_{gate} are plotted, since these are the quantities that determine the current sharing. The drain-source voltage of both units showed the same behavior already

described in Section 8.2.1 and is omitted.

Figure 8.8 shows four cycles of the supply. During conduction the two branch currents lie almost on top of one another, with peaks of 8.71 A and 8.34 A respectively; expressed in rms terms over a clean conduction window this is 5.93 A against 5.64 A, that is, a sharing imbalance of only about 5 % around a combined current of roughly 11.2 A_{rms}. Two nominally identical modules driven by a common gate command therefore share the load current well, without any active balancing, which is the result that matters for the practical use of parallelling to reach higher current ratings. At $t = 0$ the common gate command is withdrawn and both branches are extinguished together.

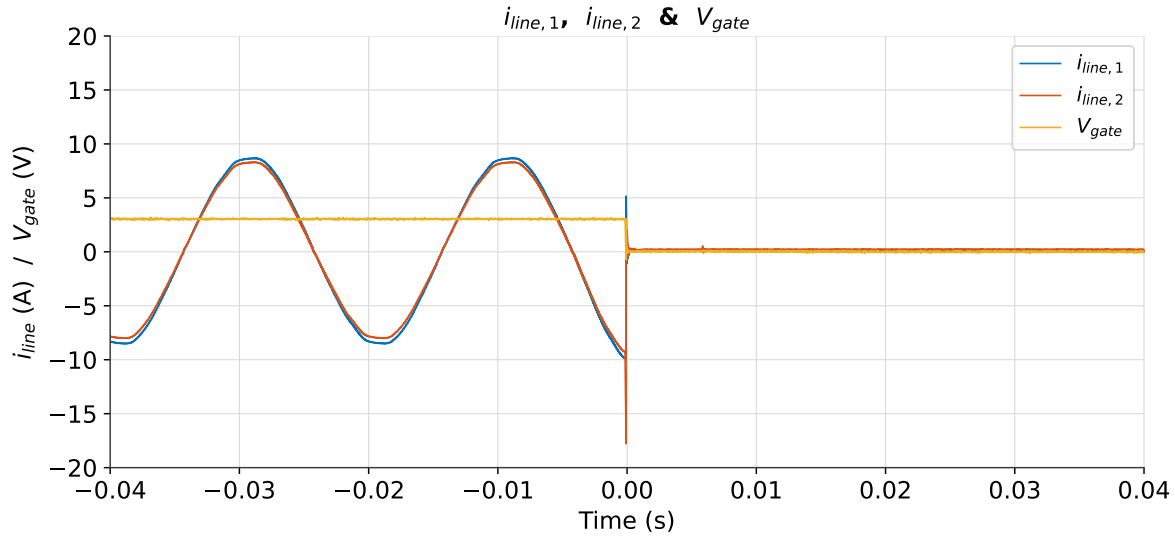


Figure 8.8. Parallel operation of two SSCB evaluation boards commanded by a common gate signal ($V = 65\,V_{rms}$, $I = 12\,A_{rms}$, software overcurrent threshold 10 A), shown over several cycles of the supply: the two branch currents and the common gate-command voltage.

The zoomed capture of Figure 8.9 shows that the good agreement observed during conduction does *not* carry over to the switching transient. Point (1) is the withdrawal of the common gate command, at which both branches are carrying approximately −9.9 A and −9.3 A; point (2), $\Delta t_1 = 55.2\,\mu$s later, is the instant at which both currents first reach zero. In between, the two branches diverge sharply: while $i_{line,1}$ swings positive to about +5.2 A, $i_{line,2}$ is driven in the opposite direction to a peak of −17.8 A, almost twice the current it was carrying before the trip. These are external branch-current measurements; they do not separately resolve the current through the main semiconductor path and the currents through the parallel snubber and clamping networks.

The observed transient sharing was sensitive to the physical interconnection: changing the length of one connecting cable between trials produced a noticeably different sharing pattern. This qualitative observation does not, however, isolate a dominant mechanism. During conduction, sharing depends on the total on-state resistance of each branch, including the devices, interconnections and contacts. During interruption, candidate contributors include unequal parasitic impedances, currents through the RC snubbers and clamping networks, and differences in the effective gate-drive waveforms

or driver delays. The board includes separate snubber and gate-drive circuitry in each module [12]; a common controller command does not establish identical local gate-to-source waveforms. Signal-integrity effects in the external command wiring are therefore another hypothesis to test, rather than a demonstrated cause of this capture.

The present measurements establish unequal external branch currents during turn-off, but do not determine the relative contributions of these mechanisms. Separating them requires simultaneous measurements of the local gate-drive and terminal voltages and controlled changes to the interconnections or snubber networks. The practical conclusion is that good steady-state sharing and a common command are insufficient to guarantee equal transient stress. Symmetric power and control interconnections and verification of the peak current stress in each module are needed when SSCB units are paralleled; neither the internal semiconductor current nor its stress can be inferred from a branch-current peak alone.

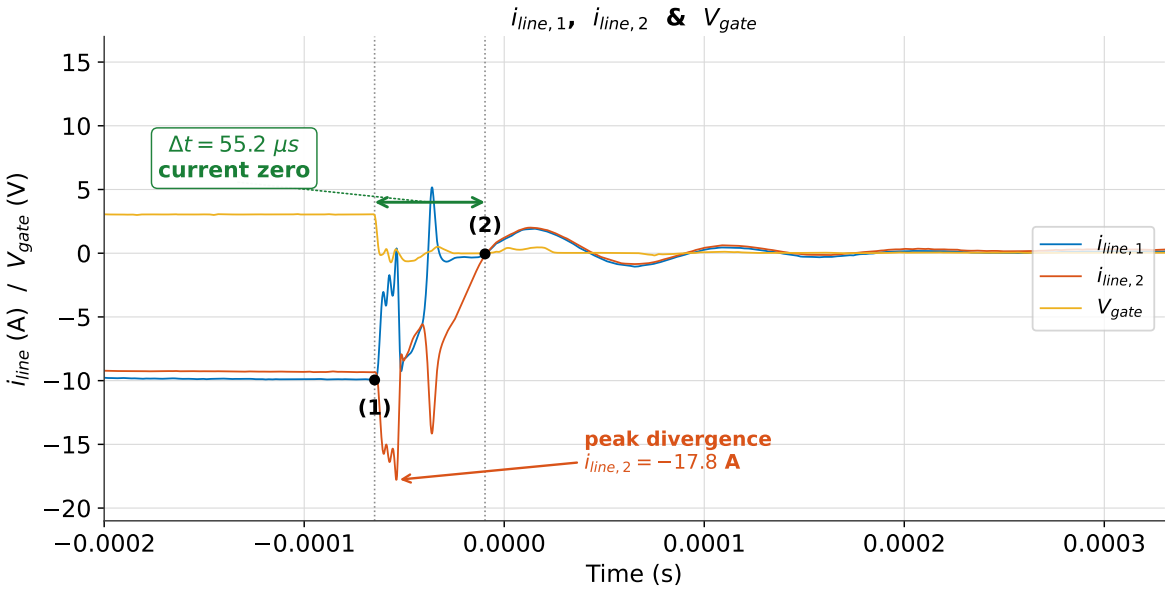


Figure 8.9. Zoomed view of the interruption of Figure 8.8. Point (1) is the withdrawal of the common gate command and point (2) the instant at which both branch currents first reach zero, $\Delta t_1 = 55.2\,\mu$s later. During the transient the two branches diverge strongly, with $i_{line,2}$ reaching -17.8 A against the -9.3 A it carried before the trip.

8.2.4 Response-time measurement

The overall response time of the SSCB, from the issuing of the trip command to the actual interruption of the current, depends not only on the intrinsic switching speed of the power semiconductors but also on the latency introduced by the control chain – in particular, in the LaunchPad-based configuration, by the discretization of the current-measurement and control loop at the PLECS simulation time step T_s. This experiment was designed to isolate and quantify this latter contribution.

Measurement procedure. The real line current was recorded simultaneously, on the same oscilloscope, through two independent channels: a reference channel, acquired directly with a current probe, and a test channel, obtained by sampling the current with the LaunchPad's ADC, processing it inside the PLECS model with a given time step T_s, and reconstructing it through the on-board DAC (the same signal path shown in Figure 8.3). Both channels were exported as full-resolution CSV traces (rather than the oscilloscope's reduced on-screen data) and analyzed in MATLAB. Since the reconstructed channel contains digital reconstruction noise, a moving-average low-pass filter was applied identically to both channels before any delay computation; this is legitimate because, if $y(t) = x(t - \tau)$ and the same linear, time-invariant filter h is convolved with each signal separately, then

$$(h * y)(t) = \int h(s)\, y(t - s)\, \mathrm{d}s = \int h(s)\, x(t - s - \tau)\, \mathrm{d}s = (h * x)(t - \tau), \tag{8.1}$$

i.e. the delay τ passes through the common filtering step unchanged, regardless of the filter's phase response, so that the filter can be used freely for noise rejection without biasing the measured delay.

The delay τ between the two channels was then extracted from the *phase difference at the fundamental frequency* of the line current. Since a pure time shift satisfies $Y(f) = X(f)\, e^{-j2\pi f\tau}$ for every frequency f, evaluating this relation at the fundamental $f_0 = 50\,\mathrm{Hz}$ gives

$$\Delta\varphi(f_0) = \angle Y(f_0) - \angle X(f_0) = -2\pi f_0 \tau \quad \Longrightarrow \quad \hat{\tau} = -\frac{\Delta\varphi(f_0)}{2\pi f_0}, \tag{8.2}$$

with $X(f)$ and $Y(f)$ obtained from a full-resolution FFT of the two recordings after applying a Hann window. This method was chosen because its resolution is not limited by the sampling period of the oscilloscope – the phase, and hence the delay, is recovered as a continuous quantity rather than as an integer number of samples – and because the line current has a very high signal-to-noise ratio precisely at 50 Hz, which is where the estimate is taken.

Results. With the communication settings (SPI clock) held fixed, the delay was measured for five values of the PLECS simulation time step T_s, spanning a 25× range:

T_s (PLECS time step)	Measured delay
20 µs	53.2 µs
50 µs	123.3 µs
100 µs	166.5 µs
200 µs	267.7 µs
500 µs	786.8 µs

These measurements are compared in Figure 8.10 with what the structure of the measurement chain predicts. Two contributions to the delay scale with the time step,

and both are standard results for sampled-data measurement and control chains: a contribution of $T_s/2$ from the zero-order-hold reconstruction performed by the DAC, which holds each new sample constant until the next one arrives, and a further contribution of $1 \times T_s$ from the one-step computational pipeline of the code-generated controller, in which a sample acquired at step n only becomes available at the output at step $n+1$. Everything else in the chain – the SPI transfer, the ADC conversion, the analog front end – is fixed by the hardware and does not depend on T_s. The expected form of the delay is therefore

$$\text{delay}(T_s) \;=\; \underbrace{\tfrac{1}{2}T_s}_{\text{ZOH}} \;+\; \underbrace{1 \cdot T_s}_{\text{pipeline}} \;+ t_0 \;=\; 1.5\,T_s + t_0, \tag{8.3}$$

with t_0 a constant hardware latency. A least-squares fit of the five measurements to this form gives

$$\text{delay}(T_s) \;\approx\; 1.50\,T_s + 18\,\mu\text{s}, \tag{8.4}$$

so that the measured slope reproduces the predicted coefficient of 1.5 to within a fraction of a percent. This agreement is the main result of the experiment: it confirms that the latency of the control chain is governed by the two sampled-data mechanisms of (8.3) and not by anything else, and it means that the delay can be predicted for any chosen time step rather than having to be measured again. The constant term of about $18\,\mu$s collects the fixed latencies of the SPI transfer and the ADC conversion, together with the residual instrumentation error of the comparison itself, since the reference channel is measured with a current probe while the test channel is read through a high-voltage differential probe on a 0–3.3 V signal.

A worst-case bound. The individual measurements scatter about (8.4) by up to some tens of microseconds, which is of the order of the instrumentation error just described, so quoting the fitted line as if it were exact would suggest a precision that the measurement does not support. For design purposes the more useful statement is an upper bound on the latency that the control chain can introduce. Every measured point satisfies

$$\text{delay}(T_s) \;\leq\; 1.5\,T_s + 50\,\mu\text{s}, \tag{8.5}$$

which is the form in which the result is best quoted: it states that the digital chain can never contribute more than one and a half time steps plus $50\,\mu$s to the response of the breaker, and it therefore allows a worst-case trip time to be computed for any chosen T_s without relying on the exact numerical values of a regression.

This measurement isolates the contribution of the digital control chain to the overall response time; as illustrated in Sections 8.2.2 and 8.2.3, the complete, processor-in-the-loop trip response of the SSCB – including current sampling, threshold detection and gate-command withdrawal – remains in the sub-millisecond range, two orders of magnitude faster than the 10.91 ms measured for the electromechanical contactor of Section 8.2.5.

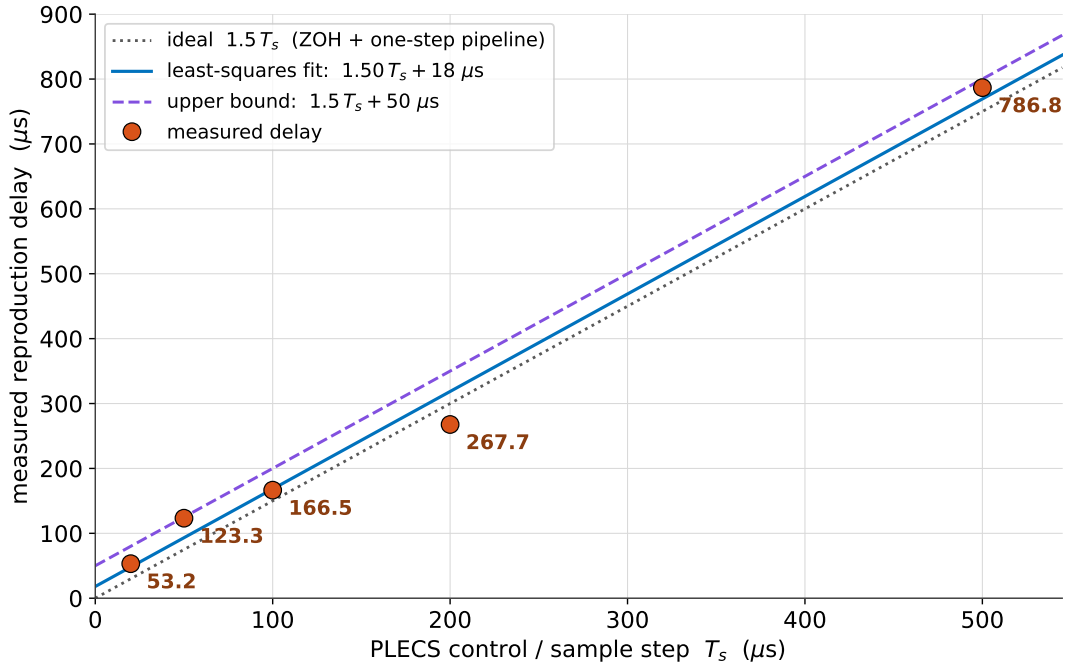


Figure 8.10. Reproduction delay of the ADC–PLECS–DAC current-sensing chain as a function of the PLECS discretization time step T_s, measured from the phase difference at the fundamental frequency. The measured points are shown together with the theoretical $1.5\,T_s$ *line, the least-squares fit* $1.50\,T_s + 18\,\mu$s *and the worst-case bound* $1.5\,T_s + 50\,\mu$s.

8.2.5 Comparison with an electromechanical contactor

Finally, in order to place the performance of the SSCB in context, the same load current ($6\,A_{rms}$ at $65\,V_{rms}$) was interrupted using a conventional electromechanical contactor in place of the SSCB, under otherwise comparable conditions, and the two recordings were then analyzed with a common procedure so that the comparison would be quantitative rather than merely visual.

The device was a Schneider Electric TeSys D LC1D09P5 three-pole contactor, of which one main pole was used to interrupt the single-phase load. The manufacturer specifies a 9 A AC-3 operational current (up to 440 V) and a 230 V, 50 Hz coil [5]. These are product ratings, distinct from the $65\,V_{rms}$, $6\,A_{rms}$ load conditions used here. The experiment compares interruption of this load; it is not a short-circuit breaking-capacity test or a characterization of all electromechanical circuit breakers.

Figure 8.11 shows the contactor interruption itself. Three signals are recorded: the voltage v_{sw} across the contactor contacts, the line current i_{line} under interruption, and the current i_{coil} in the contactor coil, which is the command signal in this case. At $t = 0$ the coil is de-energized and i_{coil} falls, so the contacts begin to separate. What follows is the essential difference from a solid-state device: the contact voltage does *not* rise to block the supply. It remains at about 1 V, because an arc strikes between the separating contacts as soon as they part and holds the circuit closed. With only a volt of arc voltage opposing it, the line current continues essentially undisturbed to the end of the half-cycle, reaching its normal peak of -8.3 A.

At $t = 7.51$ ms the current reaches its natural zero, and this is the moment at which a mechanical breaker would be expected to clear. It does not: the gap between the contacts has not yet recovered enough dielectric strength, the arc *reignites*, and current resumes in the opposite direction. What finally stops it is not a current zero but the growth of the arc voltage itself. During this second half-cycle the contacts continue to travel apart, and v_{sw} can be seen climbing steeply – roughly 39 V at $t = 10.0$ ms and 67 V at $t = 10.7$ ms – so that this rising counter-voltage progressively chokes the current, which peaks at only $+5.2$ A against the 8.3 A of the half-cycle before it. The arc becomes unsustainable at $t = 10.92$ ms, some 3.4 ms after the first current zero, and only then does v_{sw} settle at about 90 V peak and the device genuinely become an open switch.

The contactor therefore does not interrupt the current at all in the sense that the SSCB does: it separates its contacts and then waits, through a full current zero and most of a further half-cycle, until the arc can no longer sustain itself. The total clearing time of 10.91 ms is set by the mechanics of contact travel and arc extinction, not by any control decision.

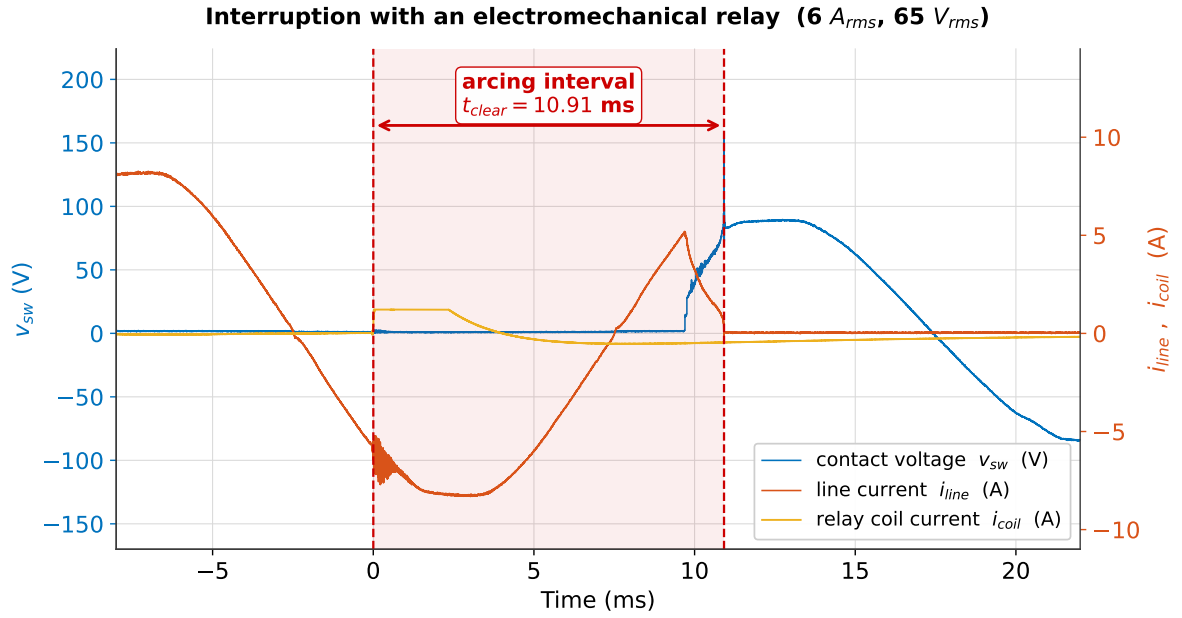


Figure 8.11. Interruption of a 6 A_{rms}, 65 V_{rms} load current with a conventional electromechanical contactor: voltage across the contactor contacts, line current and contactor coil current. The shaded band is the arcing interval, from contact separation to the final current zero.

Figure 8.12 places the two line currents side by side, both referred to their own trip command at $t = 0$. The contrast is immediate: the SSCB current has collapsed to zero before the plot has advanced appreciably from the origin, while the contactor current carries on into the negative peak of the half-cycle in which the command was issued, passes through a zero crossing without clearing, and runs on through most of a further half-cycle before the arc is finally extinguished. The two dashed lines, which mark the instant of final current zero for each device, lie at 0.139 ms and 10.91 ms respectively, a ratio of 78×. In the first few hundred microseconds after the command – the interval

over which the whole SSCB interruption of Section 8.2.2 takes place – the contactor has not reacted at all, and its current is still the undisturbed load current.

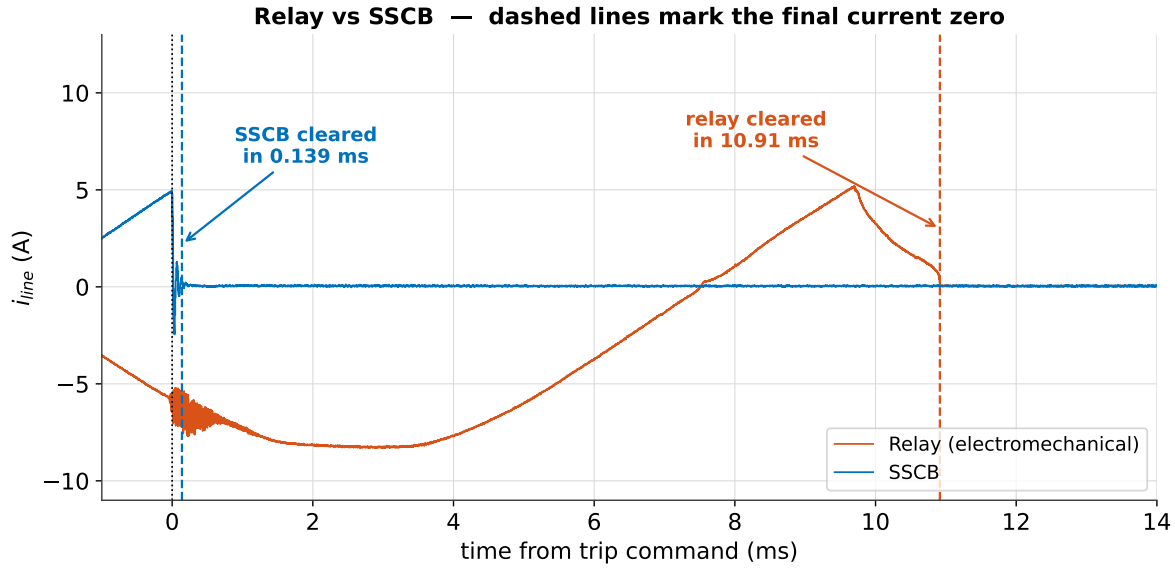


Figure 8.12. Line current during interruption of the same 6 A_{rms} load by the electromechanical contactor and by the SSCB, both referred to their own trip command at $t = 0$. The dashed lines mark the final current zero of each device.

Let-through energy. The practical consequence of this difference is best expressed through the let-through energy, that is, the quantity $\int i(t)^2 \, dt$ that the protected circuit is forced to absorb between the trip command and the final current zero. For each recording the command instant was located as the point of maximum slope of the command channel, the clearing instant as the last sample at which the current still exceeded 5 % of its pre-fault peak, and the integral was evaluated by the trapezoidal rule between the two. Applied to the two captures, this gives 0.348 A^2s for the electromechanical contactor against 3.39×10^{-4} A^2s for the SSCB (Figure 8.13): a reduction by a factor of approximately 1000.

The energy ratio ($\approx 1000\times$) is so much larger than the time ratio ($78\times$). The let-through energy scales with the integral of the *square* of the current, and the two devices do not clear at the same point of the waveform: the SSCB removes the current within microseconds of the command, while it is still well below its peak, whereas the contactor lets the current run through the whole remainder of the half-cycle, including its maximum. The solid-state breaker therefore gains twice over – once from being faster, and once from never allowing the current to reach the values that dominate the integral. For equipment with limited short-circuit withstand capability, this is the figure of merit that matters, and it is the clearest single quantitative argument in favor of solid-state protection that emerges from these experiments.

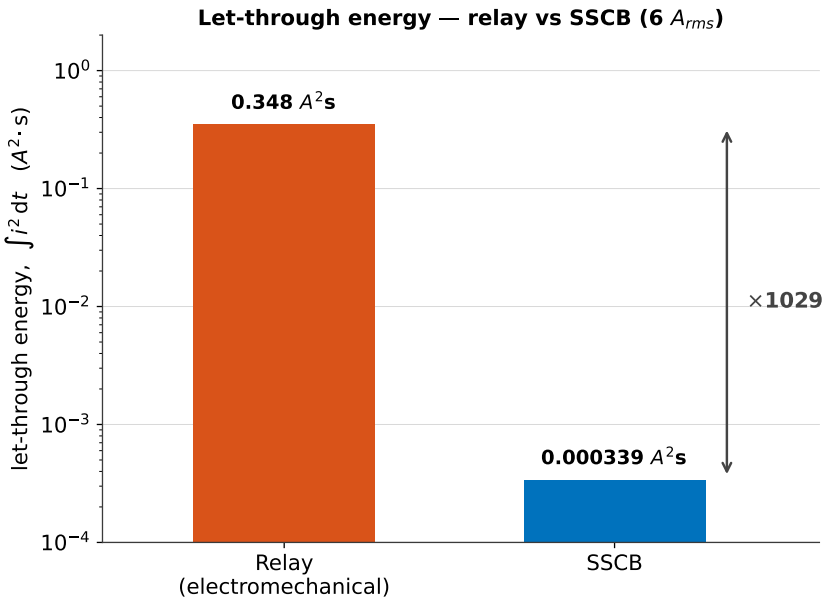


Figure 8.13. Let-through energy $\int i(t)^2\,\mathrm{d}t$ delivered during interruption of a $6\,\mathrm{A_{rms}}$ load current by the electromechanical contactor and by the SSCB, computed between the trip command and the final current zero of each device. Note the logarithmic scale.

8.3 Summary

The experiments described in this chapter provide a first hardware validation of the concepts discussed theoretically and studied in simulation in the previous chapters. Interruption with the onboard manual switch confirmed the basic conduction and blocking behavior of the evaluation board; control through the external, PLECS-programmed Texas Instruments LaunchPad confirmed that the SSCB can be reliably commanded by a processor-based controller through its external gate-command interface; the parallel connection of two units showed close current sharing between branches during conduction but a pronounced divergence during the turn-off transient, which proved sensitive to wiring asymmetries and which implies that paralleled modules must be rated for more than their nominal share of the current; a dedicated measurement isolated and quantified the latency introduced by the digital control chain as an approximately $1.5\,T_s$ function of the PLECS time step; and a direct comparison with a conventional electromechanical contactor confirmed, both in the time-domain waveforms and in the let-through energy delivered to the load, the orders-of-magnitude advantage in interruption speed that motivates the use of solid-state circuit breakers in applications with limited fault-current withstand capability.

Chapter 9

Challenges, Open Issues and Future Directions

The preceding chapters established that the solid-state circuit breaker interrupts faster than any competing technology, and quantified by how much: three orders of magnitude faster than an electromechanical breaker in simulation (Section 7.1.8) and a factor of 78 in measurement, corresponding to a reduction of the let-through I^2t by roughly three orders of magnitude (Section 8.2.5). None of this is in dispute. What prevents the technology from displacing mechanical breakers in the majority of distribution applications is a different set of quantities altogether: conduction losses, component endurance, cost, and the practical difficulty of assembling devices into a breaker of useful rating. This chapter examines each of them, drawing where possible on the specific results obtained in this work.

9.1 Conduction losses and thermal management

The on-state loss is the one figure of merit on which the electromechanical breaker remains superior by orders of magnitude, and it is the principal obstacle to wider adoption [2, 6]. Even with the most advanced SiC MOSFETs the on-state voltage drop at rated current is of the order of 1–2 V, and an AC pole places two devices in the current path. A 600 A breaker therefore dissipates 1–2 kW per pole in steady state. The comparison with the contact resistance quoted in Section 1.2 is stark: at the same current, a molded-case breaker with a contact resistance below 100 $\mu\Omega$ dissipates a few tens of watts. The solid-state breaker is thus one to two orders of magnitude less efficient in the state in which it spends essentially all of its life, and this loss must be removed as heat by an over-dimensioned heatsink or by active cooling, both of which add volume, cost and a further failure mode.

Three routes out of this constraint are being pursued. The first is device technology: the on-state resistance of wide-bandgap devices continues to fall for a given voltage class, and the migration from silicon is the single largest contributor to date [14]. The second is paralleling, which divides the current among several dies; the experiment of Section 8.2.3 shows that this works well in conduction but introduces a transient penalty of its own, discussed in Section 9.4. The third is architectural: the hybrid breaker of Section 4.2 carries the load current through a mechanical contact and inserts the semiconductor only during the interruption, which removes the steady-state loss entirely at the cost of a moving part and a more complex control sequence. Which of the three prevails is likely to depend on the application: the loss penalty is tolerable in a low-voltage feeder protecting sensitive converters, and prohibitive in a bulk distribution substation.

9.2 Endurance of the energy-absorption branch

A limitation specific to the solid-state breaker, and one that the simulation work of this thesis brought out clearly, is the finite endurance of the clamping varistor. Unlike a surge arrester, which is stressed only by rare lightning or switching events, the varistor of a breaker absorbs the magnetic energy of the network at *every* interruption and is driven into its clamping region on each operation. Repeated stress of this kind degrades the intergranular barriers, raising the leakage current in the pre-breakdown region and drifting the whole characteristic downward, as described in Section 6.4.2 [40, 42].

The quantitative consequence is that the varistor, not the semiconductor, sets the duty cycle of the breaker. In the single-phase model a direct interruption deposits approximately 14 J in the varistor; the same fault handled in current-limiting mode, with the varistor left to clamp every chopping transition, accumulates about 450 J over a 40 ms window (Section 7.1.7). A semiconductor rated for 10^6 operations is therefore paired with a component that a single current-limiting event can stress thirty times harder than a normal trip. The controlled freewheeling path proposed in that section returns the figure to approximately 12 J, but it does so by adding a rectifier bridge, a controlled switch and a dump resistor to the breaker. The alternative, a varistor specified for repetitive rather than single-shot duty [40], trades circuit complexity for component size and cost. Neither route has yet produced a standard answer, and dimensioning the energy-absorption branch, or providing for its replacement over the service life of the breaker, remains an open practical question wherever frequent operation is expected, as in microgrid reconfiguration.

A related question that this work leaves open is the three-phase case. The per-pole varistor voltages of Section 7.2.2 show that the three poles do not share the absorbed energy equally, because they interrupt at different points of their respective cycles, so each pole must be rated for the worst-case single-phase energy rather than for the mean. Quantifying that worst case over possible fault instants is a natural extension of the present model. A systematic sweep of the fault inception angle can be combined with repeated Monte Carlo simulations of component tolerances, using explicitly stated distributions and standard deviations. This would quantify the spread of per-pole energy and identify severe cases for sizing; random sampling alone would not establish an absolute worst-case bound.

9.3 Cost and standardization

The cost of a solid-state breaker is currently several times that of an electromechanical breaker of equivalent rating. The semiconductors are only part of it: the gate driver, the sensing chain, the varistor and the cooling system all scale with the rating, and production volumes remain low [2]. Commercial low-voltage products and evaluation-grade hardware are nevertheless now available from both switchgear manufacturers and semiconductor vendors [11, 12], which is the usual precondition for volume-driven cost reduction.

Standardization is the less visible half of the problem. Solid-state breakers are today qualified against standards written for mechanical devices, whose test procedures presuppose a moving contact and an arc: making and breaking capacity, mechanical endurance and dielectric withstand across an open gap. Several of these map awkwardly onto a device that has no contact, cannot provide galvanic isolation without an auxiliary disconnector, and whose endurance is limited by the thermal cycling of a package rather than by contact erosion. Conversely, quantities that are decisive for a solid-state breaker have no standardized definition: the let-through I^2t as a function of the trip threshold, the repetitive energy rating of the clamping branch, and the latency budget of the detection chain. Until these are defined, comparing products from different manufacturers on a common basis is difficult.

9.4 Scalability and series/parallel operation

Reaching useful ratings still requires several devices per pole, and this work encountered both directions of the problem. Series connection is required by voltage: the head-of-feeder location examined in Section 7.2.1 demands a pole blocking 20 kV, against the 3.3 kV of commercially mature SiC MOSFETs, and static and dynamic voltage sharing across a stack of series devices is the corresponding design problem [24, 43]. Parallel connection is required by current, and Section 8.2.3 measured what it costs. Two nominally identical modules driven by a common gate command shared the load current to within about 5 % in conduction. During the turn-off transient, however, the two branches diverged sharply, one of them carrying almost twice the current it had conducted before the trip, and the sharing pattern proved sensitive to the length of a single connecting cable.

The measurement shows that good steady-state current sharing and a common controller command do not guarantee equal transient behavior. The recorded external branch currents do not isolate the semiconductor current from the snubber and clamping currents, nor do they identify a unique cause of the imbalance. Parasitic impedances, the snubber networks and differences in local gate-drive behavior are candidate contributors, as discussed in Section 8.2.3. A paralleled solid-state breaker therefore requires attention to the symmetry of both power and control interconnections and verification of the transient stress in each module. The relative contributions of these mechanisms, and whether gate-level coordination can reduce the imbalance, remain questions for dedicated measurements.

9.5 Integration with digital protection and communications

Modern protection schemes are increasingly digital and communications-based, exchanging measurements, status and trip commands between devices in real time [8]. A solid-state breaker fits this paradigm more naturally than a mechanical one, because it is already an electronic device with a digital control system, and because its trip time

is short enough that the communication and decision latency, rather than the actuator, becomes the dominant term in the protection chain.

That shift places a new requirement on the designer, and the measurement of Section 8.2.4 illustrates it. The latency of the digital chain was found to follow $1.5\,T_s$ plus a fixed hardware term, with the two contributions traceable to the zero-order hold and to the one-step computational pipeline. Because the relationship is structural rather than empirical, the latency can be budgeted at design time for any chosen sampling period instead of being measured after the fact. Extending this kind of accounting to the full communication-assisted scheme, so that the total time from fault inception to interruption is predictable end to end, is a prerequisite for using solid-state breakers in adaptive protection of active distribution networks and microgrids.

9.6 Coordination with existing protection and reclosing

A solid-state breaker will rarely operate alone. It will sit in a protection system that also contains mechanical breakers, fuses, residual-current devices and protective relays, whose operating times differ from its own by three orders of magnitude. Selective coordination across such a spread is not a solved problem: a device that clears in tens of microseconds will always operate first, which is desirable for a downstream fault and undesirable when the fault belongs to a neighboring zone.

The speed also creates a discrimination problem that slower devices do not have. Motor starting, transformer energization and capacitor-bank switching produce current peaks comparable to moderate faults, and a breaker that trips on the instantaneous value will not survive normal operation. Two mechanisms are available. The first is waveform-based discrimination. Harmonic restraint or blocking is already used in transformer differential relays to distinguish magnetizing inrush from internal faults [21]. Applying a related criterion to an SSCB requires a suitable measurement window and validation of its decision latency; it is not an established feature of the controller tested here. Rate-of-rise information can also supplement a current threshold [39]. The second is the current-limiting mode analyzed in Section 7.1.3: because the breaker can hold the current within a prescribed band for a short interval instead of committing immediately to a trip, it can wait long enough to distinguish a genuine fault from an inrush. This is a capability that neither a mechanical breaker nor a resonant one possesses, and the results of Section 7.1.6 suggest it is thermally affordable; what the present work did not establish is how long the band can be held before the varistor, rather than the semiconductor, becomes the binding constraint.

Coordination must also respect the applicable low-voltage ride-through (LVRT) requirements of connected generation. For external faults within the required voltage–time envelope, protection settings must allow the unit to remain connected where required by the connection rules [3]. An instantaneous overcurrent trip alone does not demonstrate this compliance. If current limiting is used during the ride-through interval, the MOV must be sized for the cumulative energy of all clamping pulses over that interval, together with cooling and repetitive-pulse limits; any dump resistor

must be rated for its corresponding duty. The required ride-through duration therefore enters the energy-absorption design. The present simulations do not establish LVRT compliance.

9.7 Towards intelligent and self-powered breakers

The last direction concerns what the breaker does besides interrupting. Because it already contains sensing, a processor and a gate driver, comparatively little needs to be added for it to perform its own diagnostics, report its accumulated duty, or accept a tripping characteristic programmed remotely. Self-powered designs, which draw their auxiliary power from the protected circuit rather than from an external supply, are a particularly natural fit for normally-on devices such as the SiC JFET [35], and the Combo JFET platform used in Chapter 8 belongs to exactly that device class: it conducts with no gate-drive power and can, in principle, harvest the energy required to turn off from the fault itself.

Beyond protection, the same hardware can act as a controllable element of the network. Fault-current-limiting converters [28] and the hosting-capacity argument of Section 6.5.1 point in the same direction: a breaker that can bound the fault contribution of the source behind it may ease equipment-stress constraints, provided the limiting behavior is included in the network study and coordinated with applicable LVRT requirements. The generator study of Section 7.2.3 illustrates shorter fault-current contribution at unit level; it does not establish a network-wide increase in admissible generation.

9.8 Closing remarks

Three results of this work bear directly on the questions above. The comparison of interruption technologies under an identical fault established that the advantage of the solid-state breaker is not marginal but categorical, and that it is larger in let-through energy than in either clearing time or peak current, because the device removes the current before it approaches its peak. The varistor energy analysis established that active current limiting, which is the most attractive capability the technology offers, is incompatible with a conventional single-shot clamping branch unless the inductive energy is diverted elsewhere at each commutation. And the parallel-operation experiment demonstrated unequal external branch currents during turn-off despite good steady-state sharing and a common command. The cause was not isolated; module-level transient stress must be assessed together with the power and control interconnections and the snubber and clamping networks.

Each of these points to work that remains. A calibrated electro-thermal model covering both devices of the anti-series pair, with realistic thermal masses, would replace the qualitative temperature traces of Chapter 7 with quantitative predictions. A per-pole energy computation in the three-phase model would turn the qualitative observation of unequal varistor loading into a sizing rule. The controlled freewheeling

path, studied here only in simulation, would benefit from experimental confirmation on the same evaluation platform. And the medium-voltage configuration, retained in this thesis as a deliberately forward-looking case, will become a practical design problem as soon as series-connected wide-bandgap stacks reach the maturity that low-voltage devices have already achieved.

Bibliography

[1] X. Lyu, J. Xie, and T. E. McDermott, "Impact of inverter-based resources on grid protection: A review of negative-sequence current generation," Pacific Northwest National Laboratory, Tech. Rep. PNNL-36069, Jun. 2024. [Online]. Available: https://www.pnnl.gov/main/publications/external/technical_reports/PNNL-36069.pdf

[2] R. Rodrigues, Y. Du, A. Antoniazzi, and P. Cairoli, "A review of solid-state circuit breakers," *IEEE Transactions on Power Electronics*, vol. 36, no. 1, pp. 364–377, Jan. 2021.

[3] European Commission, "Commission regulation (EU) 2016/631 of 14 april 2016 establishing a network code on requirements for grid connection of generators," Official Journal of the European Union, L 112, pp. 1–68, 2016, fault-ride-through requirements, Articles 14–16. [Online]. Available: https://eur-lex.europa.eu/eli/reg/2016/631/oj

[4] A. M. Tsimtsios and V. C. Nikolaidis, "Setting zero-sequence compensation factor in distance relays protecting distribution systems," *IEEE Transactions on Power Delivery*, vol. 33, no. 3, pp. 1236–1246, 2018.

[5] Schneider Electric, *TeSys D LC1D09P5: Three-Pole Contactor, 9 A AC-3, 230 V 50 Hz Coil*, Schneider Electric, product specifications, accessed 21 October 2026. [Online]. Available: https://www.se.com/gr/el/product/LC1D09P5/

[6] A. Q. Huang, "Power semiconductor devices for smart grid and renewable energy systems," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2019–2047, Nov. 2017.

[7] Z. J. Shen, "Ultrafast solid-state circuit breakers: Protecting converter-based AC and DC microgrids against short circuit faults," *IEEE Electrification Magazine*, vol. 4, no. 2, pp. 70–72, Jun. 2016.

[8] S. Mirsaeidi, X. Dong, S. Shi, and D. Tzelepis, "Challenges, advances and future directions in protection of hybrid AC/DC microgrids," *IET Renewable Power Generation*, vol. 11, no. 12, pp. 1495–1502, 2017.

[9] ABB SACE, *Electrical Installation Handbook: Protection and Control Devices; Electrical Devices*, 4th ed., ABB SACE, Mar. 2006, volumes 1 and 2. [Online]. Available: https://library.e.abb.com/public/7a93440e8c790852c125716c0033f7a9/1SDC010002D0204.pdf

[10] R. Xu, "SiC MOSFET based SSCB for aviation system applications," Ph.D. dissertation, Department of Engineering, Durham University, United Kingdom, Aug. 2024.

[11] ABB, "Solid-state circuit breaker concept," Press release, Hannover Messe, Apr. 2019, available at https://new.abb.com/news/.

[12] onsemi, *Combo JFET SSCB Evaluation Board User's Manual*, Semiconductor Components Industries, LLC, Jun. 2025, rev. 3.

[13] X. Song, C. Peng, and A. Q. Huang, "A medium-voltage hybrid DC circuit breaker, part I: Solid-state main breaker based on 15-kV SiC emitter turn-off thyristor," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 278–288, Mar. 2017.

[14] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 5, pp. 2155–2163, May 2014.

[15] J. Keller and B. Kroposki, "Understanding fault characteristics of inverter-based distributed energy resources," National Renewable Energy Laboratory, Tech. Rep. NREL/TP-550-46698, Jan. 2010. [Online]. Available: https://docs.nrel.gov/docs/fy10osti/46698.pdf

[16] International Renewable Energy Agency, "Renewable capacity statistics 2026," IRENA, Abu Dhabi, Tech. Rep., 2026.

[17] L. Rubino, G. Rubino, P. Marino, and L. P. D. Noia, "Smart solid-state circuit breaker for photovoltaic power plants," *International Review of Electrical Engineering*, vol. 12, no. 5, pp. 442–451, 2017.

[18] Q. C. Zhong and T. Hornik, *Control of Power Inverters in Renewable Energy and Smart Grid Integration*. John Wiley & Sons, 2013.

[19] A. Maqsood and K. Corzine, "DC microgrid protection: Using the coupled-inductor solid-state circuit breaker," *IEEE Electrification Magazine*, vol. 4, no. 2, pp. 58–64, Jun. 2016.

[20] F. Liu, W. Liu, X. Zha, H. Yang, and K. Feng, "Solid-state circuit breaker snubber design for transient overvoltage suppression at bus fault interruption in low-voltage DC microgrid," *IEEE Transactions on Power Electronics*, vol. 32, no. 4, pp. 3007–3021, Apr. 2017.

[21] A. Guzman, H. Altuve, and D. Tziouvaras, "Power transformer protection improvements with numerical relays," in *CIGRE Study Committee B5 Colloquium*, Calgary, Canada, Sep. 2005. [Online]. Available: https://selinc.com/api/download/3184/?lang=en

[22] N. A. Liaskos, "Analysis and design of medium-voltage direct-current circuit breakers based on resonance circuits," Master's thesis, National Technical University of Athens, Jul. 2019, in Greek.

[23] C. Peng, X. Song, A. Q. Huang, and I. Husain, "A medium-voltage hybrid DC circuit breaker, part II: Ultrafast mechanical switch," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 289–296, Mar. 2017.

[24] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid HVDC breaker: An innovation breakthrough enabling reliable HVDC grids," ABB Grid Systems Technical Paper, Tech. Rep., Nov. 2012.

[25] B. J. Baliga, *Fundamentals of Power Semiconductor Devices*, 2nd ed. Springer, 2019.

[26] P. Tielens and D. Van Hertem, "The relevance of inertia in power systems," *Renewable and Sustainable Energy Reviews*, vol. 55, pp. 999–1009, Mar. 2016.

[27] B. Kroposki, B. Johnson, Y. Zhang, V. Gevorgian, P. Denholm, B.-M. Hodge, and B. Hannegan, "Achieving a 100% renewable grid: Operating electric power systems with extremely high levels of variable renewable energy," *IEEE Power and Energy Magazine*, vol. 15, no. 2, pp. 61–73, Mar. 2017.

[28] P. Cairoli, R. A. Rodrigues, and H. Zheng, "Fault current limiting power converters for protection of DC microgrids," in *IEEE SoutheastCon*, 2017.

[29] STMicroelectronics, *How to Select the Right Thyristor (SCR) for Your Application*, STMicroelectronics, application note AN4608. [Online]. Available: https://www.st.com/resource/en/application_note/an4608-how-to-select-the-right-thyristor-scr-for-your-application-stmicroelectronics.pdf

[30] Infineon Technologies, *IGBT Characteristics*, Infineon Technologies, application note AN-983. [Online]. Available: https://www.infineon.com/dgdl/Infineon-IGBT_Characteristics-AN-v01_00-EN.pdf?fileId=5546d462533600a40153559f8d921224

[31] H. Grüning, *IGCT Technology — A Quantum Leap for High-Power Converters*, ABB Switzerland, n.d. [Online]. Available: https://library.e.abb.com/public/d627aeaa2f9f8b24c1256f4100480fa0/PT_IGCT.pdf

[32] V. Barkhordarian, *Power MOSFET Basics*, International Rectifier, n.d., application note AN-1084; hosted by Infineon Technologies. [Online]. Available: https://www.infineon.com/assets/row/public/documents/24/54/infineon-power-mosfet-basics-article-en.pdf

[33] B. Xiao, Y. Lu, and X. Hu, "Characterization of AC solid-state circuit breaker based on SiC MOSFET device," in *IEEE Conference on Industrial Electronics and Applications (ICIEA)*, 2024.

[34] Infineon Technologies, *Understanding and Interpreting the CoolSiC MOSFET 1200 V Datasheet*, Infineon Technologies, Jul. 2026, application note AN2025-10, version 1.1, 15 July 2026. [Online]. Available: https://www.infineon.com/assets/row/public/documents/60/42/infineon-an2025-10-understanding-and-interpreting-the-coolsic-mosfet-1200v-datasheet-applicationnotes-en.pdf

[35] Z. Miao, G. Sabui, A. M. Roshandeh, and Z. J. Shen, "Design and analysis of DC solid-state circuit breakers using SiC JFETs," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 863–873, Sep. 2016.

[36] Z. J. Shen, Z. Miao, A. M. Roshandeh, P. Moens *et al.*, "First experimental demonstration of solid state circuit breaker (SSCB) using 650V GaN-based monolithic bidirectional switch," in *2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, 2016, pp. 79–82.

[37] B. Sun, *Quick-Reference Guide to Driving CoolGaN GIT HEMTs 600 V: RC Interface*, Infineon Technologies, Dec. 2021, application note AN_2107_PL52_2108_141427, version 1.1. [Online]. Available: https://www.infineon.com/assets/row/public/documents/regions/singapore/infineon-rc-interface.pdf

[38] L. Balogh, *Fundamentals of MOSFET and IGBT Gate Driver Circuits*, Texas Instruments, Oct. 2018, application report SLUA618A, revised October 2018. [Online]. Available: https://www.ti.com/lit/ml/slua618a/slua618a.pdf

[39] Z. Wang, X. Shi, L. M. Tolbert, B. J. Blalock, and B. Ozpineci, "A di/dt feedback-based active gate driver for smart switching and fast overcurrent protection of IGBT modules," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3720–3732, Jul. 2014.

[40] TDK Electronics AG, *SIOV Metal Oxide Varistors: General Technical Information*, TDK Electronics AG, 2018. [Online]. Available: https://www.tdk-electronics.tdk.com/download/531268/8954d4a78154a9da5c70a7119fa03e86/siov-general.pdf

[41] K. A. Corzine, "A new-coupled-inductor circuit breaker for DC applications," *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1411–1418, 2017.

[42] Vishay BCcomponents, "Varistors — introduction," Vishay Intertechnology, Technical Note 29079, 2013, rev. 04-Sep-13.

[43] C. Peng, A. Q. Huang, and X. Song, "Current commutation in a medium-voltage hybrid DC circuit breaker using 15-kV vacuum switch and SiC devices," in *IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 2244–2250.

[44] D. Mavridis, S. Fountoukidis, and N. Papanikolaou, "Solid-state circuit breakers for renewable energy units," in *CIGRE Greece 2025 Athens Session, B5 Protection and Control in Networks with Unconventional Sources*, Athens, Greece, 2025.